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A MAGIC TOUCH:

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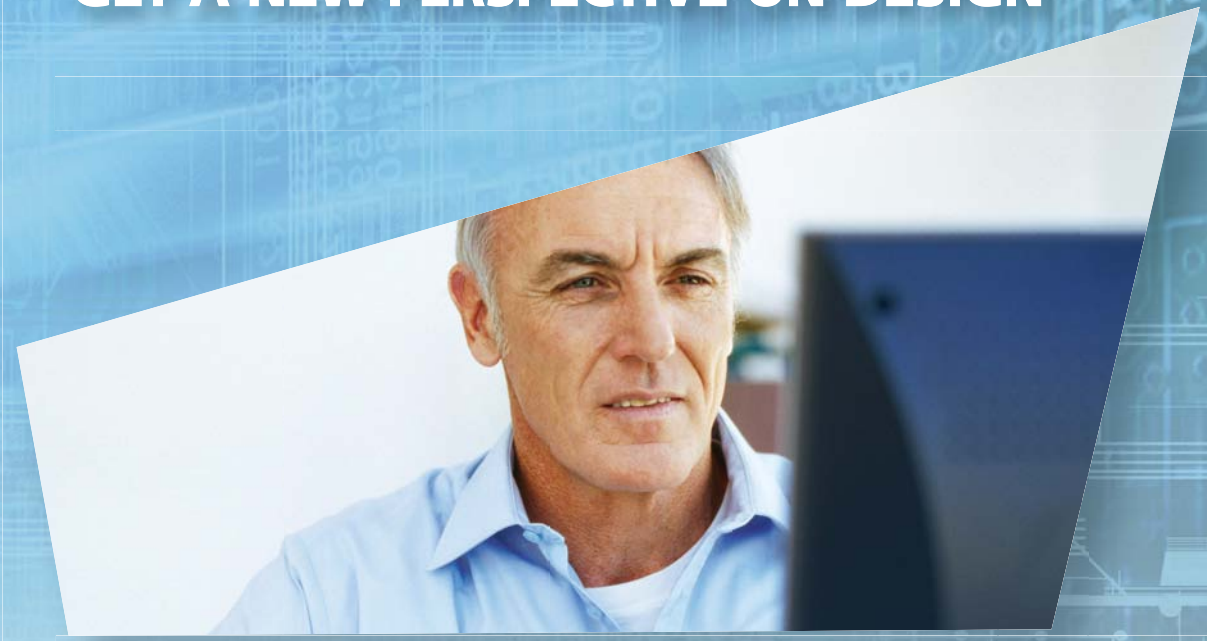

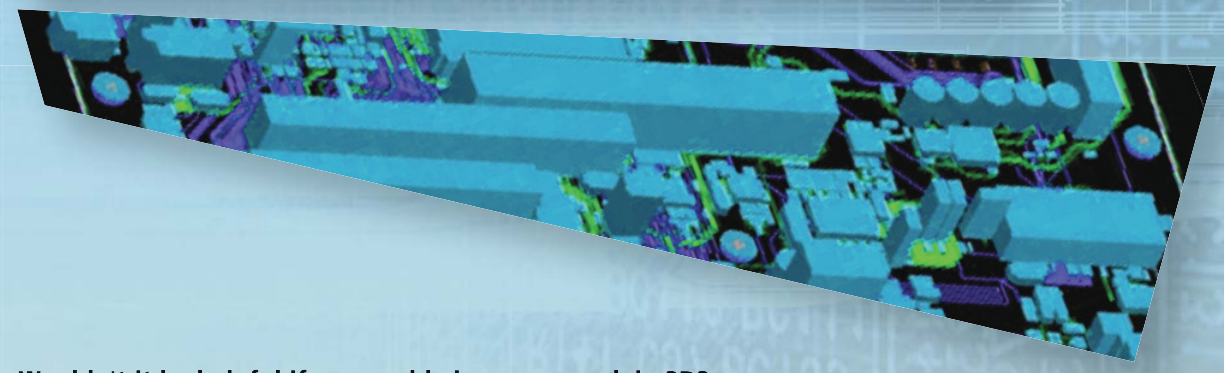

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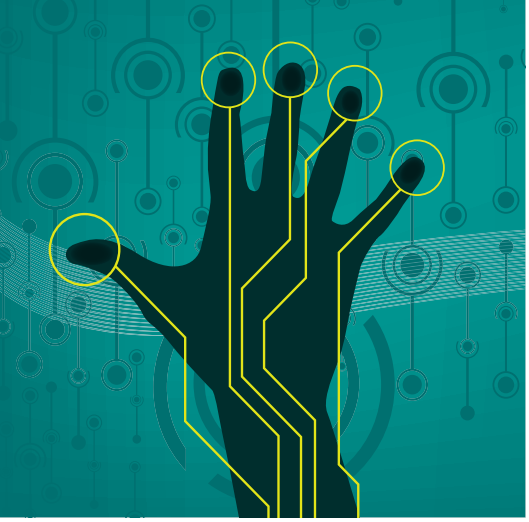

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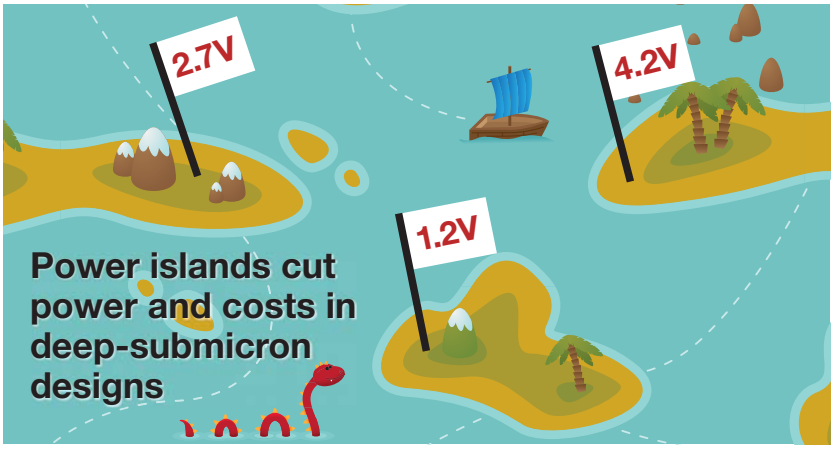
A magic touch: The concept's sound, but implementation options abound

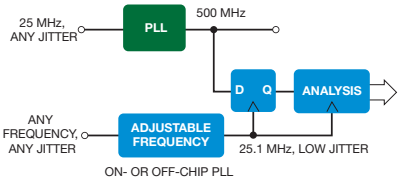
by Brian Dipert, Senior Technical Editor



Power islands cut power and costs in deep-submicron designs

by Martin Rosicky and Mark Barry, S3 Group

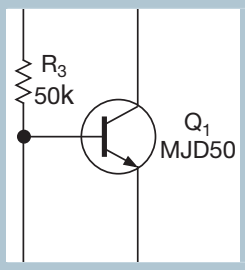
pulse



Essential principles for practical analog BIST

by Steve Sunter, Mentor Graphics

DESIGNIDEAS



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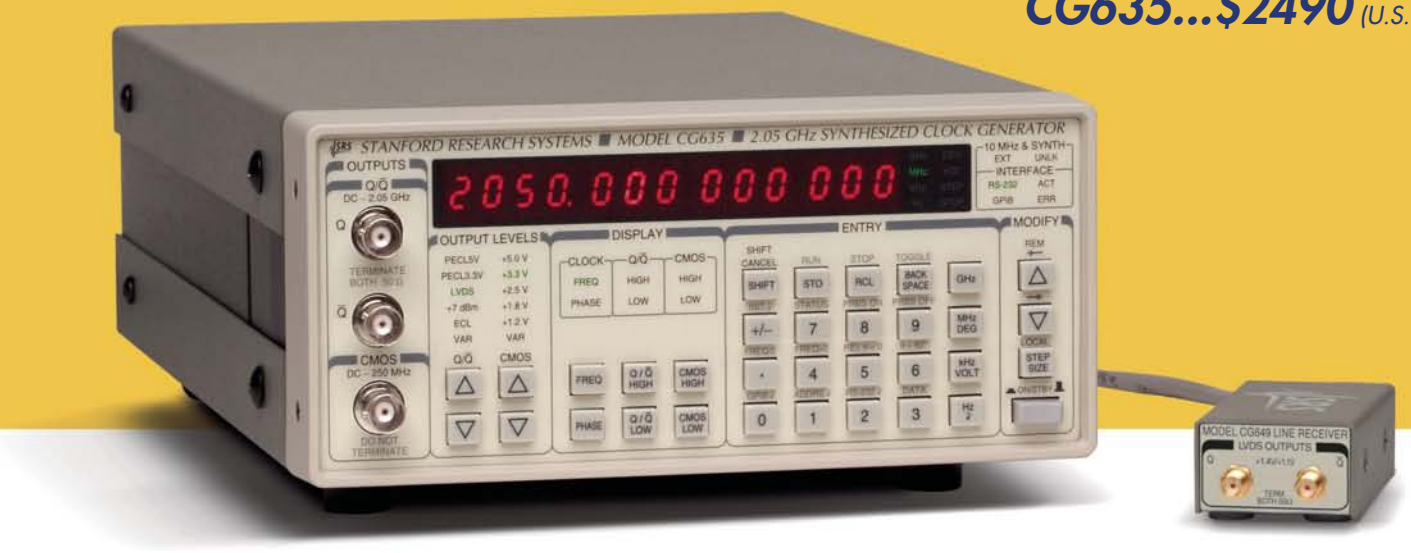
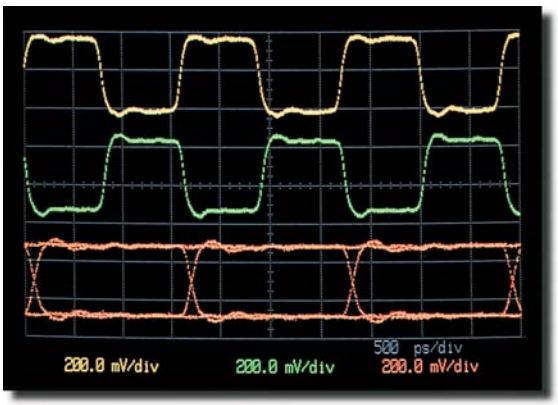


- ***Square wave clocks from DC to 2.05 GHz***
- ***Random jitter <1 ps (rms)***
- ***80 ps rise and fall times***
- ***16-digit frequency resolution***
- ***CMOS, LVDS, ECL, PECL, RS-485***
- ***Phase adjustment & time modulation***



Plot shows complementary clocks and PRBS (opt. 01) outputs at 622.08 Mb/s with LVDS levels. Traces have transition times of 80 ps and jitter less than 1 ps (rms).

The CG635 generates clock signals—flawlessly. The clock signals are fast, clean and accurate, and can be set to standard logic levels.

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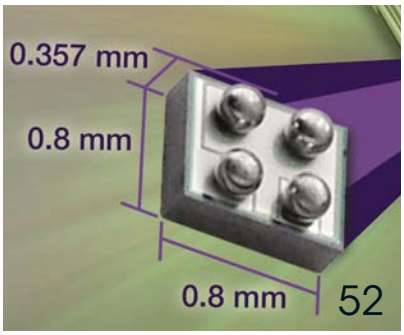

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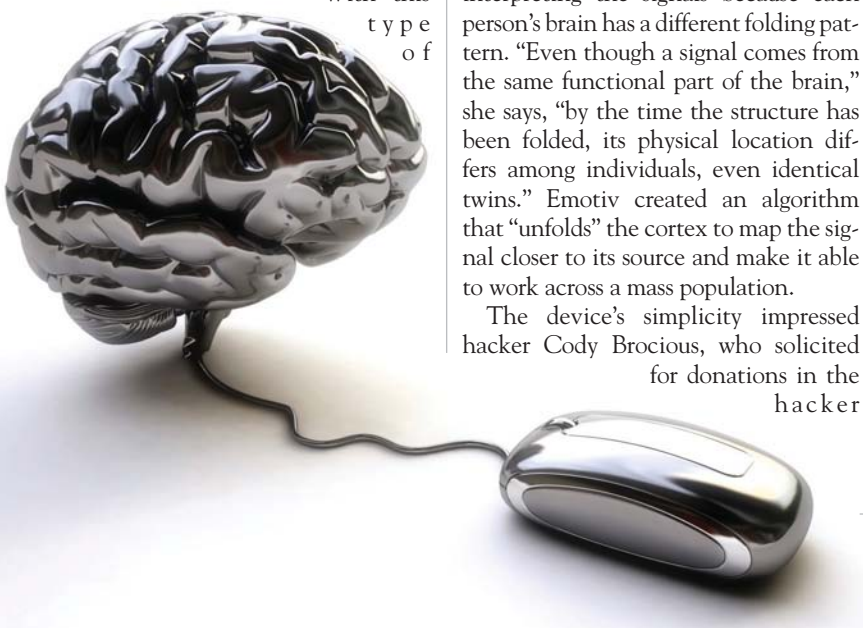
BY MARGERY CONNER, TECHNICAL EDITOR

To hack the brain, you need to hack the hardware

The human body—especially the brain—may be the final frontier for hackers. The same curiosity that drives users to open applications, see what makes them tick, and then improve or repurpose them is even more relevant for the brain. Equipment to monitor the brain and its responses is expensive, limiting research into BCIs (brain-to-computer interfaces) to academia and medical research. However, the gaming market, in which thought control of games is a novel gimmick, is driving the appearance of BCI devices at prices far lower than the tens of thousands of dollars you can expect to pay for medical-research-quality EEG (electroencephalography), which records the electrical activity along the scalp that the firing of neurons within the brain produces. (For more on BCIs, see next issue's cover story, "Brain-to-computer-interface hardware moves from the realm of research.")

A new headset, the Emotiv Epoc, sells for approximately $300 and is simple to use: Pull it from the box, connect it to your PC, place it on your head, spend a few moments on the canned exercises that let the headset algorithms learn your brain-wave pattern, and you can begin manipulating virtual images on your PC with your brain. With this type of gear, it becomes feasible to hack your own brain.



The headset combines hardware and sophisticated algorithms that analyze and interpret the tiny EEG voltages. According to Emotiv founder Tan Le at a recent TED (technology/entertainment/design) conference, the folds of a brain present a significant challenge in interpreting the signals because each person's brain has a different folding pattern. "Even though a signal comes from the same functional part of the brain," she says, "by the time the structure has been folded, its physical location differs among individuals, even identical twins." Emotiv created an algorithm that "unfolds" the cortex to map the signal closer to its source and make it able to work across a mass population.

The device's simplicity impressed hacker Cody Brocious, who solicited for donations in the hacker community and quickly raised the funds to buy a headset. He discovered the key to the encrypted data coming over the USB (Universal Serial Bus) connection and built a decryption routine. So far, his library of code hacks to the device just pulls raw data from the unit; it can't filter the signals or tell which sensor corresponds to each data stream. Brocious created Cody's Emokit project, an open-source library for reading data directly from the headset, and posted research about his project on the Emotiv user forum, which the company runs (**Reference 1**).

Emotiv officials didn't like the fact that Brocious cracked the encryption and posted his library, claiming that doing so could force the company out of business (**Reference 2**). Emotiv sells a $700 developers' version of the headset that allows access to the data, but it is not an open environment; the company controls access. Apparently, the company is working to close the encryption hole and end the project.

Emotiv must choose whether and how to protect its business model. It might do well to take a look at a recent announcement from Amazon about its creation of an app store for Android phones (**Reference 3**). Amazon sees how lucrative the growing market is for apps that run on the open Android standard—perhaps more profitable than selling the phone itself. Emotiv could be better off in opening the headset interface and encouraging the headset as an open-standard platform. Besides the elegance of the headset, the company's secret sauce seems to be filtering algorithms, which would not be part of an open hardware interface. EDN

REFERENCES

1 Emokit. GitHub Social Coding, http://bit.ly/b1W09O.
2 "Raw Emotiv signals encryption hacked on consumer headset," http://bit.ly/crLtgO.
3 Kane, Yukari Iwatani, and Geoffrey A Fowler, "Amazon Amps Up Apps Rivalry," *The Wall Street Journal*, Oct 7, 2010, http://bit.ly/axtym6.

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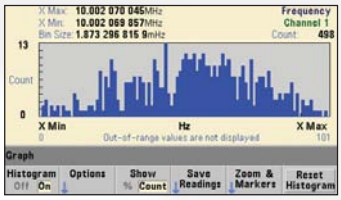

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INNOVATIONS & INNOVATORS

FloTherm 9 addresses thermal bottlenecks

Mentor Graphics has announced its next-generation FloTherm 3-D CFD (computational fluid-dynamics) software for electronics-cooling applications. Erich Bürgel, general manager of Mentor's mechanical-analysis division, says that the patent-pending technology in the FloTherm 9 software provides Bn (bottleneck) and Sc (short-cut) fields so that, for the first time, engineers can identify where and why heat-flow congestion occurs in electronic design. The software also identifies thermal short cuts to help quickly resolve design problems.

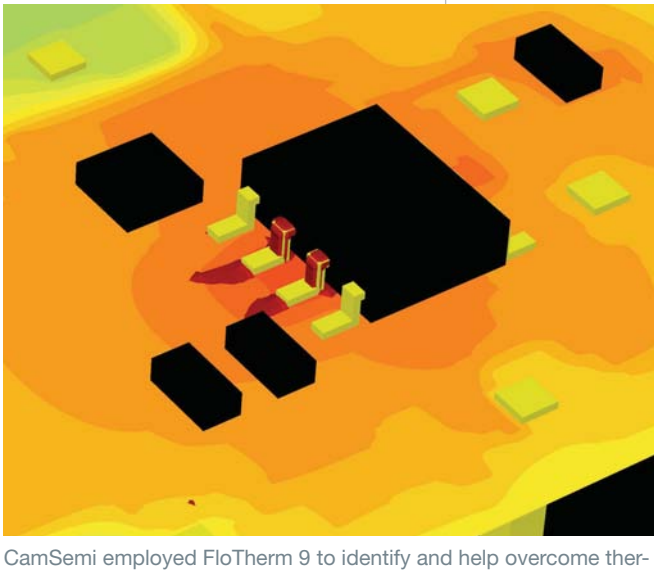
The Bn and the Sc fields convert the software from an observation tool, which identifies heat-management problems, to an effective thermal-design-problem-solving tool that suggests potential solutions to the designer. Bürgel says that CamSemi (www.camsemi.com) has used the software as a thermal-design tool.

According to Nigel Heather, vice president of engineering at CamSemi, FloTherm 9 saved the company time and cost when developing an IC for a new generation of Energy Star-compliant mobile-phone chargers. "The baseline simulation using the bottleneck feature quickly highlighted a potential thermal issue, and further iterations confirmed our solution," he says. "To achieve the same result by building prototype boards would have taken a long time and drawn resources away from other critical work."

Bürgel explains that the Bn field shows where in a design the heat path is being congested as it attempts to flow from high-junction-temperature points to the ambient. Design changes to these bottlenecks can help solve the heat-flow problem. The Sc field highlights possible approaches, in which the addition of a simple element, such as a gap pad or chassis extrusion, provides a new effective heat-flow path to further cool the system.

FloTherm 9 supports the importing of XML (Extensible Markup Language) model and geometry data to enable the integration of FloTherm into data flows. Version 9 also has a direct interface to the Mentor Graphics Expedition PCB (printed-circuit-board)-design platform. The direct interface enables users to import native Expedition PCB data and delete or edit additional objects, such as heat sinks, thermal vias, board cutouts, and electromagnetic cans, for more accurate thermal-model-design development. **—by Rick Nelson**

▷**Mentor Graphics**, www.mentor.com/products/mechanical/products/flotherm.



CamSemi employed FloTherm 9 to identify and help overcome thermal bottlenecks when it designed an IC for a mobile-device charger.

TALKBACK

"The lawmakers run strictly on emotion and appealing to the masses without a lot of facts getting in the way. It has been that way for quite a few years, and I really don't see any means of changing it."

—Engineer and writer William Ketel, in *EDN*'s Talkback Section, at http://bit.ly/cWTI4M. Add your comments.

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Bypass-diode replacement shuts down solar-panel hot spots

Solar panels usually find use in multiple-unit configurations—whether on residential rooftops with a dozen panels or a utility solar farm with thousands of panels. These arrays need protection from panel failures or shading; otherwise, 8 to 12A in a string of panels has nowhere to go.

Panels traditionally rely on a simple bypass diode to shunt current around a failed panel. STMicroelectronics has introduced a more sophisticated controller-switch SIP (system in package), which replaces the bypass diode with a more intelligent device. The SPV1001 contains a low-loss power switch and a precision controller and eliminates almost all of the energy each diode loses when the panel is producing energy and the diode is in its off state. For example, reverse-leakage current at 40V reverse voltage is 1 µA at 25°C and 20 µA at 125°C. The forward-voltage drop at a forward current of 8A is 70 and 160 mV at 25 and 125°C, respectively.

The SPV1001 contains a low-loss power switch and a precision controller and eliminates almost all of the energy each diode loses when the panel is producing energy and the diode is in its off state.

The device comprises a power MOS transistor that charges a capacitor during the off time and drives its gate during the on time with the charge it previously stored in the capacitor. On and off times reduce the average voltage drop across the drain and source terminals and thus their power dissipation. The SPV1001 sells for approximately $3 (1000), depending on the package.

—by Margery Conner

▷**STMicroelectronics**, www.st.com.

AMD GPUs tout performance as high as 2 TFLOPS

AMD (Advanced Micro Devices) has unveiled the first two members of its second-generation DX11-supportive family, the Radeon HD 6000 series of GPUs (graphics-processing units). Both the HD 6850 and 6870 use a 40-nm process and have 1.7 billion transistors. Engine clocks run at 725 and 900 MHz, respectively, and computation performance is 1.5 and 2 TFLOPS (trillion floating-point operations/sec), respectively. The 6850 has 960 system processors, and the 6870 has 1120, and peak power consumption is 127 and 151W, respectively.

The 6850 sells for $179 in board form with a 1-Gbyte frame buffer. The 6870 sells for $229, also with 1 Gbyte of GDDR5 (graphics double-data-rate 5) SDRAM. Both chips interface to their frame-buffer memory arrays over a 256-bit bus and embed a dual DVI and a dual mini DisplayPort interface, along with an HDMI (high-definition-multimedia-interface) port. The 6870-based boards require two six-pin power connectors; the 6850 boards require only one. **—by Brian Dipert**

▷**AMD**, www.amd.com.

DILBERT By Scott Adams

TI OFFERS FREE WINDOWS EMBEDDED CE 6.0 R3 BSPs

11.04.10

Texas Instruments has introduced Microsoft Windows Embedded CE 6.0 R3 BSPs (board-support packages) for OMAP (open multimedia applications platform)-L1x floating-point DSP and ARM9 processors, Sitara AM1x ARM9 microprocessors, and associated evaluation modules. For OMAP-L1x, the BSP provides access to TI's TMS320C674x DSP using DSP/BIOS Link interprocessor-communication software, enabling you to develop algorithms using CE 6.0 R3. Download these BSPs from www.ti.com/wincebsp-prtf.

The OMAP-L1x and AM1x BSPs are compatible with the OMAP-L137, OMAP-L138, AM1707, and AM1808 processors; the AM17x, AM18x, and OMAP-L138/TMS320C6748 evaluation modules; the AM18x and OMAP-L138 experimenter's kits; and the OMAPL137/C6747 floating-point starter kit. TI plans to expand its list of Windows CE-supported product lines. These products will include the Sitara AM3517 and AM3505, the DaVinci DM644x video processors, and several OMAP35x devices. CE 6.0 R3 BSPs for OMAP-L1x and AM1x devices are available at www.ti.com/wincebsp-prtf.

—by Rick Nelson

▷Texas Instruments, www.ti.com.

Wake-up receiver offers 15- to 150-kHz range

Austriamicrosystems has introduced the three-channel AS3933 low-frequency receiver, which enables battery-powered systems to add remote-wake-up capability. It offers a sensitivity of 80 ⊠V rms with current consumption of only 2.7 ⊠A to extend battery life.

Featuring a receiver frequency range of 15 to 150 kHz, the AS3933 can serve applications including active RFID, high-value asset tracking, real-time-location systems, operator identification, wireless sensor networks, and access control or remote keyless entry.

The AS3933 provides a digital RSSI (received-signal-strength-indicator) value for each active channel, and it supports a programmable data rate and Manchester decoding with clock recovery. It also includes an internal clock generator derived from either a crystal oscillator or the internal RC oscillator. According to the company, it is the first such device to provide a built-in automatic antenna tuner that tunes the antenna to the desired carrier frequency. Customers frequently request this feature to reduce their BOM (bill-of-materials) costs without compromising cost.

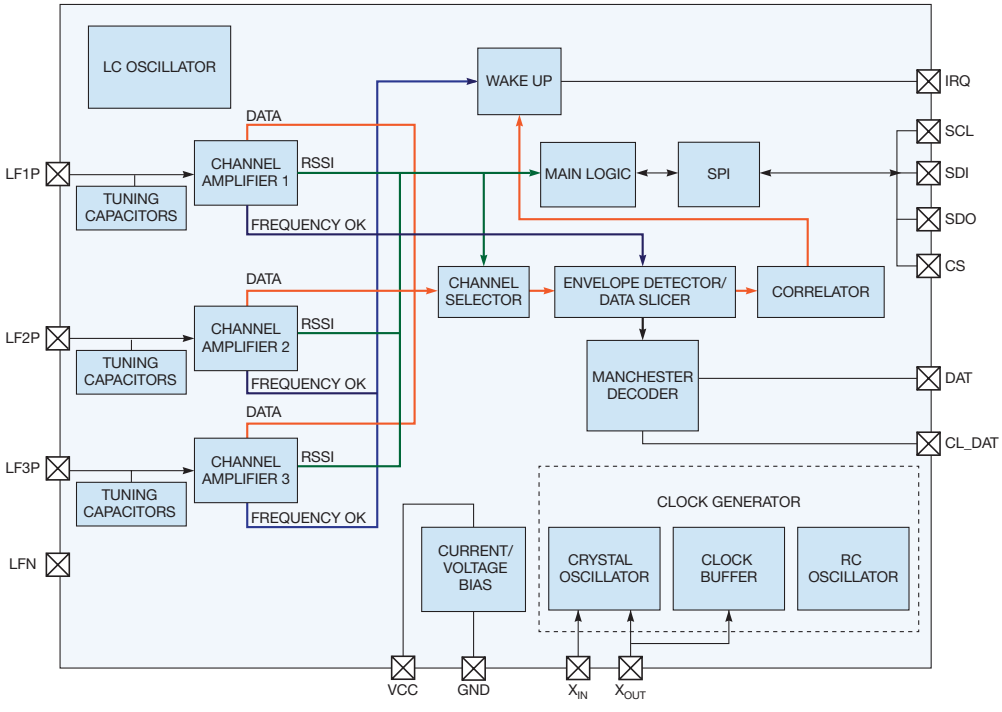
The programmable features of the AS3933 allow optimized settings for longer operating distance and retain reliable wake-up generation. You can adjust the AS3933's sensitivity level in the presence of a strong RF field or in noisy environments. The automatic-tuning feature ensures perfect matching to the desired carrier frequency, simplifying antenna tuning.

The AS3933 also features reliable 1-, 2-, or 3-D wake-up-pattern detection and supports wake-up without pattern detection. It has an adjustable sensitivity level, is resistant to false wake-ups, and has a false-wake-up counter. Dynamic range is 64 dB, and it operates from a supply voltage of 3.4 to 3.6A at an ambient temperature of 25°C.

The AS3933 operates with a 3V power supply and over the –40 to +85°C temperature range. The device is available in 4×4-mm, 16-pin TSSOP and 16-pin QFN packages. The price is $2.60 (1000), and a demonstration board is also available.

—by Rick Nelson

Austriamicrosystems, www.austriamicrosystems.com.



The three-channel AS3933 receiver supports Manchester decoding and includes an internal clock generator derived from either a crystal oscillator or the internal RC oscillator.

11.04.10

16-BIT, 250M-SAMPLE/SEC ADC SERVES SEVERAL APPLICATIONS

Analog Devices' new 16-bit, input-buffered AD9467 pipeline ADC can attain an SNR (signal-to-noise ratio) of 76.4 dB full-scale and an SFDR (spurious-free dynamic range) of 100 dB full-scale. The device operates from 1.8 and 3.3V rails and consumes 1.32W when operating at 250M samples/sec. Jitter is 60 fsec rms. It has LVDS (low-voltage-differential-signaling) outputs on eight multiplexed pairs of pins providing the 16-bit output. The ADC suits use in military radar, data-acquisition systems, cell-phone base stations, power-amplifier linearization, infrared imaging, and antenna-array positioning. The differential analog input has 3.5-pF equivalent input capacitance and 530Ω input resistance. You can program the full-scale input range at 2 to 2.5V, allowing a trade-off between SNR and SFDR. Analog Devices provides behavioral models of the device that reproduce errors associated with both static and dynamic features.

The part comes in 72-pin LFCSPs, operates over a –40 to +85°C temperature range, and has a suggested retail price of $120 (1000). The AD0467-250EBZ evaluation board costs $300.

—by Paul Rako

Analog Devices, www.analog.com.

100G-sample/sec real-time scope interleaves ADCs to reduce noise

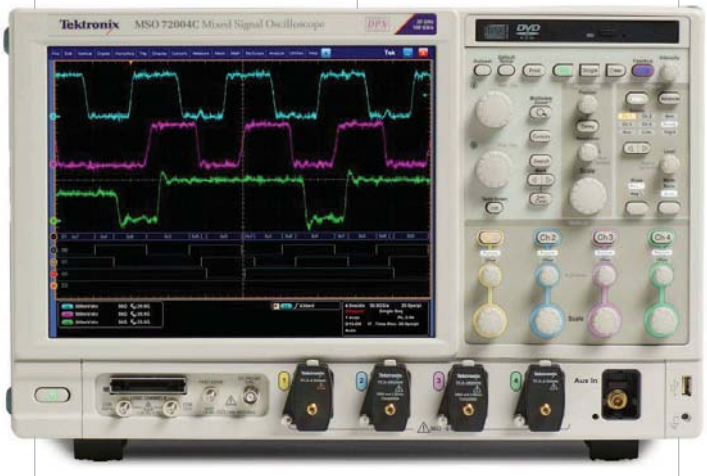
Tektronix has announced the DPO (digital-phosphor-oscilloscope), DSA (digital-signal analyzer), and MSO (mixed-signal-oscilloscope) 70000C series, which simultaneously capture 100G samples/sec on two channels or 50G samples/sec on four channels. The higher sampling rate yields lower noise and increased numbers of data points on five-times-oversampled 20-GHz waveforms. MSO models also include 16 logic-timing-analysis channels that each acquire 12.5G samples/sec.

According to the company, the five-times oversampling is the highest of any high-bandwidth real-time scope. It delivers significant benefits, including more accurate signal-integrity measurements for such high-speed serial standards as PCIe (Peripheral Component Interconnect Express) 3. Other enhancements include a faster computing platform and a more stable timebase, ideal for radar applications.

You can use high-performance oscilloscopes with bandwidths greater than 4 GHz in a variety of high-speed-serial, wideband-radar, fast-optical-communications, high-end embedded-system, and high-energy-physics applications. As designs move to ever-higher data rates, the measurement system's margin becomes increasingly critical. The new series delivers the performance and signal fidelity designers need to ensure that their latest components and systems meet design specifications.

Besides the twofold increase in sampling rate compared with the B series it replaces, the C series features a computing platform that offers faster processing of longer data records, such as those in jitter, noise, and BER (bit-error-rate) measurements and statistics. Booting and application start-up are also significantly quicker.

In any digital oscilloscope, there is a strong correlation between sampling rate and internal noise. A high sampling rate results in less noise, which in turn increases the user's margin. Extensive comparison testing shows that the C series operating in the 100G-sample/sec, two-channel mode delivers as much as 20% less noise than does the same instrument operating in the 50G-sample/sec, four-channel mode.



Most high-performance real-time digital scopes gain bandwidth when they interleave pairs of channels' ADCs and capture memory to double the sampling rate. The units in the 70000C series, such as this 20-GHz-bandwidth MSO72004C, in contrast, gain time resolution and SNR (signal-to-noise ratio).

Modern radar designs use frequency and phase modulation within the radar pulses to improve range-resolution and target-identification capabilities. Maintaining the same modulation characteristics from pulse to pulse is key to the system's operation. High-performance oscilloscopes are the tools of choice for radar-pulse measurement but must have a stable timebase that stays on frequency for long captures. The DPO/DSA/MSO70000C series meets this requirement with a new high-stability timebase that reduces long-term jitter, phase, and frequency instability. With the pulse- and frequency-settling-measurement capabilities of Tektronix's SignalVu vector-signal-analysis software, the C series enables designers of frequency-agile radios and radars to accurately verify system performance.

The DPO/DSA/MSO70000C scopes provide the bandwidth and sampling rates for debugging serial-data signals to 12 Gbps on all four channels simultaneously—ideal for multilane applications, including PCIe 3, SATA (serial advanced-technology attachment), 6-Gbps SuperSpeed USB (Universal Serial Bus), HDMI (high-definition multimedia interface), DisplayPort, and 10-Gbps Ethernet. The FastAcq acquisition mode provides a capture rate greater than 300,000 waveforms/sec—about 100 times as fast as competing alternatives—delivering both critical insight into signal behavior and in-depth analysis.

> Probing accessories enable both analog and digital connections to the device under test with minimal disruption.

Tektronix offers a range of software packages for high-speed serial-data design, debugging, and compliance verification. These packages include DPOjet for jitter and timing analysis; SDLA (serial-data-link analysis) for testing transmitters, interconnects, and receivers; and standard-specific packages for DDR, DisplayPort, PCIe, USB, HDMI, SATA, Ethernet, Fibre Channel, and others. In addition, Tektronix delivers a variety of oscilloscope probing accessories, including TriMode probes, for making both analog and digital connections to the device under test with minimal disruption. US prices for the DPO/DSA/MSO70000C series start at $110,000 for a 12.5-GHz-bandwidth DPO71254C.

—by Dan Strassberg

▷**Tektronix Inc**, www.tek.com.

Analog Devices: enabling the designs that make a difference in people's lives

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ANALOG DEVICES

BY HOWARD JOHNSON, PhD

Time invariance

"According to the Western science you value so highly, time itself eventually comes to an end," said my friend Chris "Breathe" Frue, a talented musician and audio technician who wants to learn more about equalizers, a subject pertaining to both audio and high-speed digital systems. "Nothing can remain time-invariant for *all time*."

"Maybe it would help to look at a circuit that is *not* time-invariant," I replied. "Let's say the power-supply ripple-filter capacitors in an old tube amplifier were to dry out and start to fail. The dc-power voltage available to the tubes would develop large, 60-cycle undulations. You would probably hear a lot of hum in the output."

"My old keyboard amp did that," said Breathe.

I continued, "Besides the hum, the gain of the amplifier actually varies, along with the 60-cycle variations in power voltage, causing a high-speed tremolo effect. A quick experiment to measure the gain on just 10 cycles of a 4000-Hz burst would return different results depending on precisely where within the 60-cycle hum pattern the experiment began. In contrast, a time-invariant system behaves the same regardless of when, within a reasonable span of time, you begin your experiment. Even if the time-invariant system already produces a certain amount of inherent delay, if you delay the input by a certain time, you delay the output by that much more."

In response to Breathe's request for an example, I said, "A hard-limiting, or clipping, function is perfectly time-invariant. It distorts your signal through an instantaneous process that happens point by point. Time doesn't matter."

"So, a good amplifier with no hum would be time-invariant?" he asked.

"Pretty much," I answered. "Two key properties we look for in any audio system are superposition and time invariance **[Reference 1]**. Given those properties, the system can process any combination of signals, at any time, just as well as an individual signal."

Breathe knit his brow. "You said 'just as well as.' That sounds like an important caveat."

"It is," I agreed. "What processes do you know so far that obey superposition and time invariance?"

"Well, the clipping function you just mentioned is time-invariant but does not obey superposition," he said. "A tremolo circuit probably obeys superposition but varies its gain with time. The only process I know that satisfies both properties is a simple scaling factor."

"One other process," I replied, "satisfies both properties: a time delay. Think about it. Scaling and delay, and linear combinations of different amounts of scaling and delay, are the only things you can do that obey both superposition and time invariance. These simple operations form the basis of almost all forms of equalization."

"Delay and scaling are such simple operations," said Breathe. "Isn't that restrictive?"

"It's wonderfully restrictive," I answered. "The requirements of time invariance, coupled with superposition, weed out a tremendous number of ineffective functions, leaving the rich array of possible system operations generally known as linear operations, or, more precisely, linear-time-invariant operations. For example, take signal $x(t)$ and subtract from it a slightly delayed version of the same signal." On a paper napkin, I wrote $y(t)=x(t)-x(t-\Delta t)$.

Staring at the napkin, Breathe said, "That looks like the definition of the time-derivative from calculus."

"Yes, it does," I said. "For small values of Δt (change in time), it looks almost exactly the same. The time-derivative operator from calculus and the act of integration over time are both linear, time-invariant processes. Integration is just a cumulative, running sum of previous values of a signal. So scaling, delay, differentiation, and integration are the basic processes that are both linear and time-invariant."

"If I remember my circuit theory correctly, a typical passive, linear circuit comprises a bunch of derivative and integration operations all mixed together," said Breathe. "Does this mean that all passive, linear electronic circuits are linear-time-invariant processes?"

"You got it!" I answered. "All passive, linear circuits do the 'same thing.' They just apply some linear-time-invariant process to the input signal. The big questions are, Which processes do they apply? And how do we characterize what those processes do?" EDN

REFERENCE

1 Johnson, Howard, "Linear superposition," *EDN*, Oct 7, 2010, pg 21, http://bit.ly/bOXC7g.

LINEAR TECHNOLOGY

DESIGN NOTES

Convert Temperature to Current at High Linearity with LT3092 Current Source – Design Note 484

Todd Owen

Electronics 101

One of the first lessons in a basic electronics course covers the symbols for resistors, capacitors, inductors, voltage sources and current sources. Although each symbol represents a functional component of a real-world circuit, only some of the symbols have direct physical counterparts. For instance, the three discrete passive devices—resistors, capacitors, inductors—can be picked off a shelf and placed on a real board much as their symbolic analogs appear in a basic schematic. Likewise, while voltage sources have no direct 2-terminal analog, a voltage source can be easily built with an off-the-shelf linear regulator.

The black sheep of basic electronics symbols has long been the 2-terminal current source. The symbol shows up in every basic electronics course, but Electronics 101 instructors must take time to explain away the lack of a real-world equivalent. The symbol presents a simple electronics concept, but building a current source has, until now, been a complex undertaking.

A Real 2-Terminal Current Source

With the introduction of the LT®3092, it is now as easy to produce a 2-terminal current source as it is to create a voltage source. Figure 1 shows how the LT3092 uses an internal current source and error amplifier, together with the ratio of two external resistors, to program a constant output current at any level between 0.5mA and 200mA.

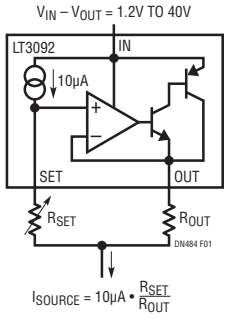

Figure 1. 2-Terminal Current Source Requires Only Two Resistors to Program

The flat temperature coefficient of the internal reference current (highlighted in Figure 2) is as good as many voltage references. Low TC resistors do not need to be used; the temperature coefficients of the external resistors need only match one another for optimum results.

No frequency compensation or supply bypass capacitors are needed. Frequency compensation is internal and the internal reference circuitry is buffered to protect it from line changes.

No input-to-output capacitors are required. While extensive testing has been done to ensure stable operation under the widest possible set of conditions, complex load impedance conditions could provoke instability. As such, testing in situ with final component values is highly recommended. If stability issues occur, they can be resolved with small capacitors or series RC combinations placed on the input, output, or from input to output.

The LT3092 offers all the protection features expected from a high performance product: thermal shutdown, overcurrent protection, reverse-voltage and reverse-current protection. Because a simple resistor ratio sets the current, a wide variety of techniques can be utilized to adjust the current on the fly. The LT3092 can also be configured as a linear regulator without output capacitors for use in intrinsic safety environments.

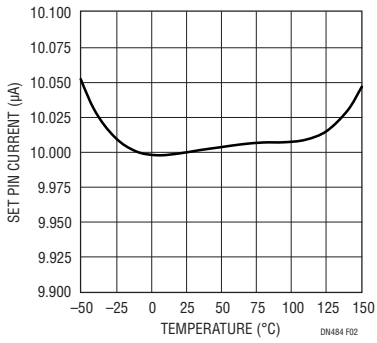

Figure 2. SET Pin Current vs Temperature

The LT3092 as a T-to-I Converter

Omega's 44200 series linear thermistor kits* include thermistors and resistors that together create a linear response to temperature when appropriately configured. These kits generate either a voltage or resistance proportional to temperature with high accuracy; the #44201 kit is listed for the 0°C to 100°C temperature range with 0.15°C accuracy.

Obviously, these kits easily satisfy the needs of a wide variety of applications, but problems arise when the thermistor must be placed at the end of a long wire—application information from Omega suggests no more than 100 feet of #22 wire for thermistor kit #44201. Wire impedance interferes with the thermistor resistance and defeats the accuracy inherent in the kit.

By adding the LT3092 to the thermistor kit along with three 0.1% accuracy resistors and one final trim, a very accurate 2-terminal temperature-to-current converter can be built. This circuit measures 700µA operating current at 0°C, dropping by 2µA every degree until 100°C, at which point the current measures 500µA. The obvious advantage to this T-to-I converter over a T-to-V converter is that current remains constant regardless of the wire length—as long as there is sufficient voltage to meet the compliance of the LT3092 circuit while not exceeding its absolute maximum. Electronics 101: Kirchoff's laws dictate conservation of current in the wire runs as long as there are no nodes for current to leak along the run.

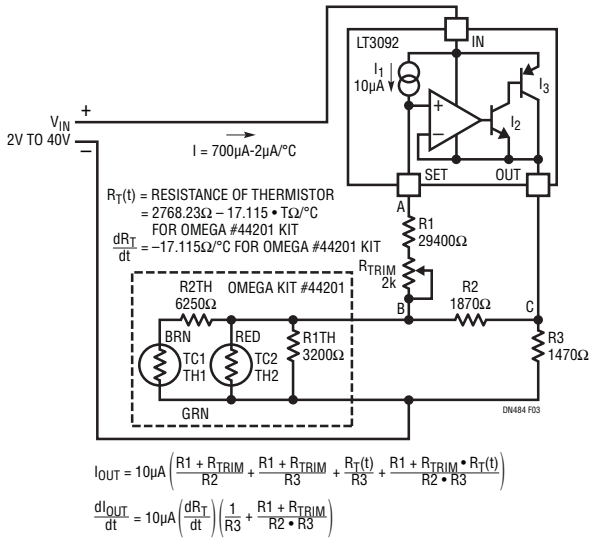

Figure 3. 2-Terminal Temperature-to-Current Thermometer Suitable for Use at the End of Long Wire Runs

Data Sheet Download

www.linear.com

Figure 3 shows the schematic for linear thermistor kit #44201 from Omega with the LT3092 and the additional resistor values. The formulas under the figure allow for substitution of other thermistor kit values and determination of appropriate complementary resistors to fit the application.

Once the initial circuit is built, any initial tolerance, variations, and offsets are easily trimmed out by connecting a voltmeter from node A to node B and trimming the potentiometer to measure 302mV (for this design). This voltage remains constant regardless of temperature.

Now, one wire runs out and back for temperature sensing at significant distances. By providing input voltage above the compliance level of the LT3092 (less than 2V for this circuit and resistor combination) and sensing the resultant current (use a 1k resistor and DVM) one can measure temperature. Figure 4 shows the current output from the circuit across temperature and the difference between measured and calculated response.

Conclusion

The LT3092 requires only two external resistors to produce a 2-terminal current source that references to input or ground, or sits in series with signal lines.

A 2-terminal current source enables a number of applications, especially those involving long wire runs, as Kirchoff's laws dictate the conservation of current over long wire distances—distances where a voltage signal would be corrupted. The example presented here uses the LT3092 and a linear thermistor kit to convert temperature to current, creating a 2-terminal current output thermometer. Placing this in series with long distances of wire maintains accuracy despite the distance of wire used.

*Available from www.omega.com

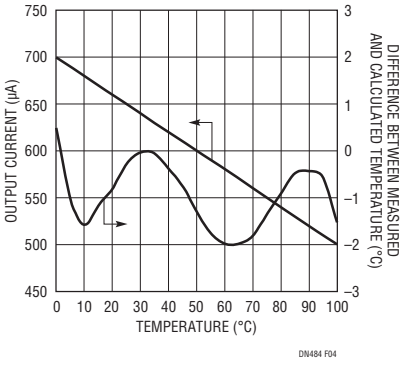

Figure 4. Calculated vs Measured Performance of the Thermometer in Figure 3.

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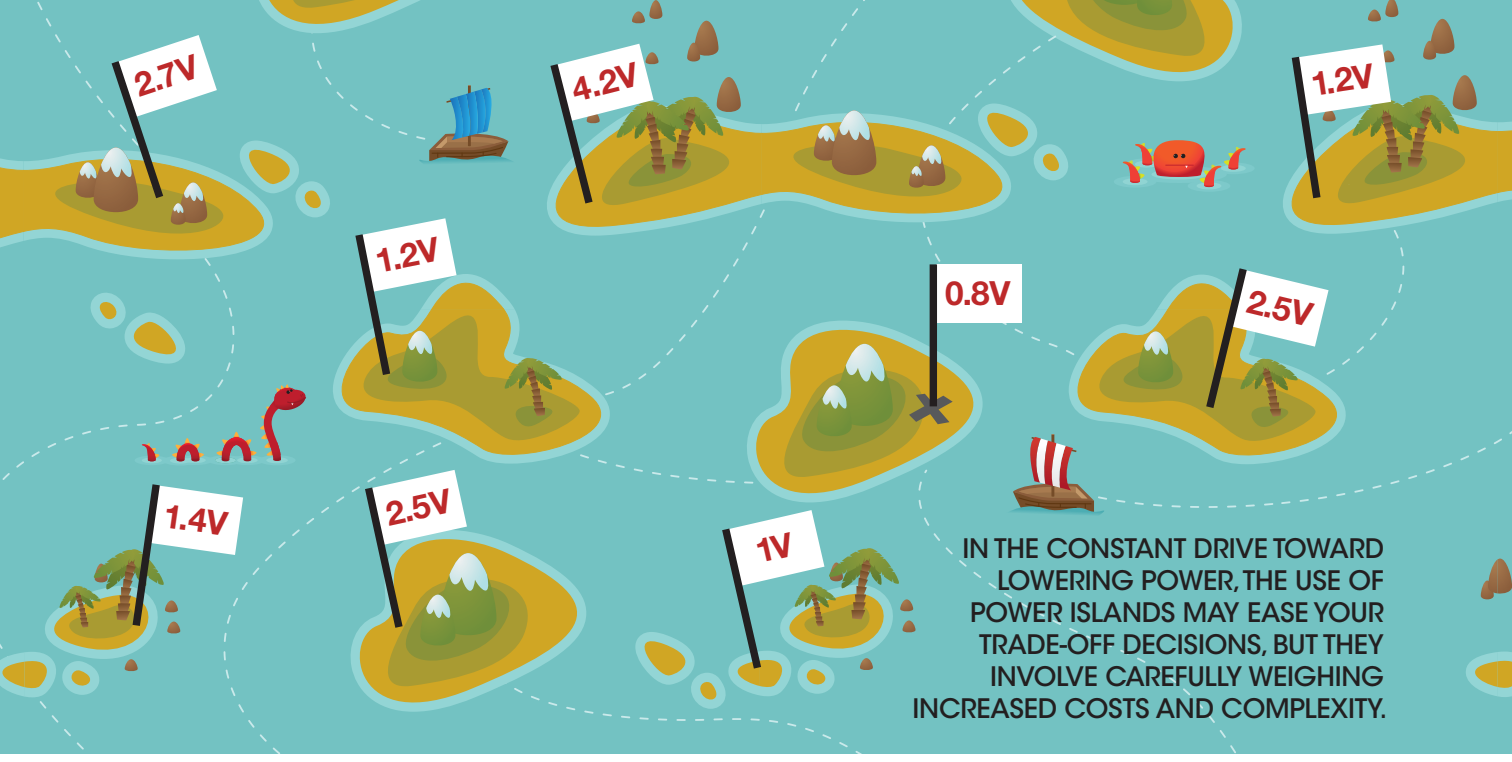

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POWER ISLANDS
CUT POWER AND COSTS IN DEEP-SUBMICRON DESIGNS

BY MARTIN ROSICKY AND MARK BARRY • S3 GROUP

Today's imperative to reduce power in both mobile and mains-powered devices is forcing engineers to search for cost-effective ways to reduce power consumption in their designs. Voltage scaling and voltage gating are useful approaches for reducing dynamic and leakage power. Adding power islands to a product may seem like a no-brainer in the race to beat your competitors. However, your decision to do so may become more difficult if this step adds several years' worth of engineering effort, delays tape-out, and adds to your die's cost.

Although many techniques exist for reducing power consumption, the most common approach for today's deep-submicron designs is to implement power islands. The implementation of power islands yields substantial returns on investment, from reducing packaging and cooling costs to increasing revenues and margins due to longer battery life and longer product lifetime. These considerations have a large impact on your profits.

WHY USE POWER ISLANDS?

Increasing levels of integration and the availability of deep-submicron technologies result in opportunities for innovative power management. Power consumption itself is important, particularly in battery-operated devices. However, increasing power density is also important. Pay close attention to this parameter because failure to do so can damage the device or dramatically shorten its lifetime. Power management is a must for most designs implemented in technologies smaller than 90 nm.

Both static- and dynamic-power consumption are proportional to the power-supply voltage. Power voltage scaling and voltage gating are among the most effective power-saving methods. However, for performance reasons, it is sometimes impossible to reduce voltage for the whole device, and performance requirements of some parts of the design can differ dramatically.

Typically, most of the peripherals can operate at a lower frequency than that of the chip core. The full voltage supply that a high-performance core requires is often unnecessary for its peripheral blocks (**Figure 1**). Moreover, various blocks spend a substantial amount of

time in idle mode. Therefore, you can achieve huge power savings by reducing or even switching off power for low-performance and idle blocks. To separately handle the power supply for blocks, you must split the design into power islands. Such intervention requires careful analysis, planning, and implementation, which result in inevitable overhead costs.

WHAT IS THE COST?

You must consider many factors when deciding whether to implement power islands. For one thing, they require a more costly architecture and specification phase. Techniques for handling power islands range from the simplest voltage gating of domains to the highest-performance dynamic voltage and frequency scaling. Each technique results in power savings with correspondingly different costs and risks. Your choice of a power-saving technique depends on your application, the technology, and the risk inherent to power-control implementations. Engineers thus must carefully analyze the design during an architectural study phase to explore these variants and propose an optimal design. The output of the study should cover expected power savings and the associated cost and risks. This architectural analysis requires additional NRE (nonrecurring-engineering) costs. It comprises not only the technical staff's effort but often also the EDA-tool-license costs. This support is unavoidable in many cases and may even require expensive ESL (electronic-system-level)-tool licenses for architectural exploration. The tools can enable and substantially speed selection of the most effective approach for your design and verify the accuracy and completeness of the power intent. Skimping during this phase or using inappropriate tools can negatively affect NRE costs and risks later in the program.

AT A GLANCE

- Power islands provide opportunities for reducing power consumption but involve increased risks, complexity, and costs.
- Using power islands results in a more costly architecture and specification phase and significant NRE (nonrecurring-engineering) cost during implementation.
- Consider the impact of power islands on all design tasks.
- Minimize the number of power domains and the need for dynamic-power adjustment.

Splitting your design into power domains yields more modes for functional verification, static-timing analysis, layout optimization, physical validation, and design for test. This step in itself increases the runtime of all design steps and raises demands on computational power, memory allocation, and data storage. Increasing the number of input- and output-data combinations results in higher demands on data management. Moreover, new tasks appear due to the introduction of power islands. For example, you must design and verify transitions between power modes (**Figure 2**), including designing and verifying a digital-power-management block that controls power-voltage sources, clock and reset generation, power switches, state retention, and other power structures.

Power-mode-transition sequences can be complex. It is essential to create comprehensive test cases for functional verification and constraints for optimization and timing closure of these various power modes and transitions. Although EDA tools are available to support these tasks, these modes require significant NRE costs for additional RTL (register-transfer-level) design, verification, physical design, and timing closure, including setup of automated flows. Because power modes and sequencing are complex, this step can add risk to the program, compromising core functions and requiring a re-spin.

Using power islands can also increase the cost of power-supply generation. Certain power-saving techniques require multiple voltage levels or levels that can

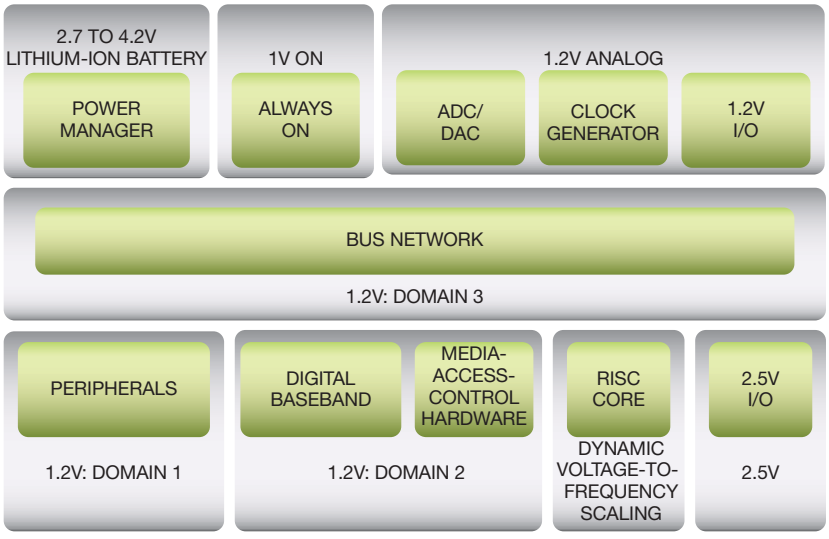

Figure 1 This IC architecture uses multiple power domains and techniques.

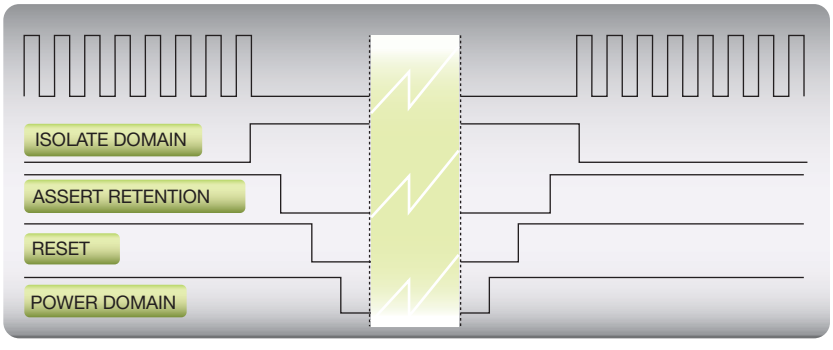

Figure 2 Even the simplest power-down of a domain requires digital control.

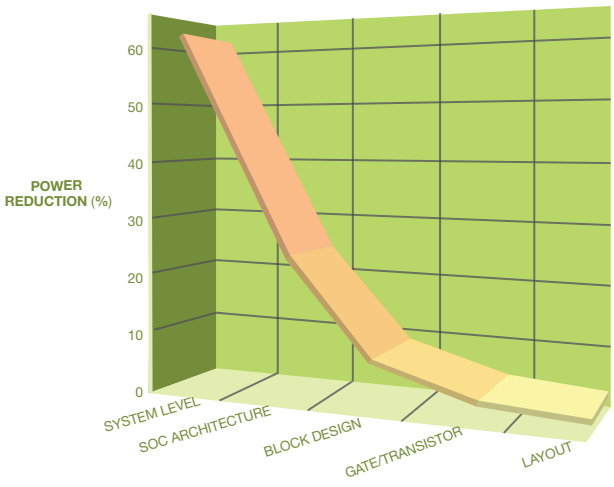

Figure 3 You'll find the largest power reductions early in the design process.

vary with time. The dc/dc converters or linear regulators that supply these additional voltage levels are complex analog blocks. If you intend to integrate these blocks on your IC, consider either the time and effort their design will require or the cost of an IP (intellectual-property) license. The likelihood of purchasing silicon-proven IP exactly matching the needs of your design in the given technology is minimal, and the IP provider typically must customize the IP according to your requirements.

A more complex power source also means an increase in the per-unit cost. For example, a dc/dc converter supplying 400 mA of current may add 7 cents to the die costs in a 65-nm process and potentially push you into a more costly package with more pins to supply the additional 10% or so of current the converter itself loses. Not integrating IP and going instead for an external power-management IC can cost from 1 cent for the addition of a rail to an existing power-management unit to $1.50 to buy a new dc/dc IC supplying that 400 mA. Additional external components, such as capacitors and inductors, are also necessary, pushing up the BOM (bill-of-materials) cost by a couple of cents, adding to OEM-integration NRE costs, and reducing board reliability.

Precision and early power estimation require additional NRE costs. You must base the requirements of the power sources on power-consumption estimates. A power source driving more current than necessary will require more die area and may result in a larger per-unit cost. Too weak a power source is simply a disaster and may result in functional failure. You must consider the additional NRE costs, including EDA-tool costs, for the power-consumption estimation in an appropriate design phase. Early estimations are less precise; however, a late start on the power-source design can endanger the program schedule.

Power-management structures imply area overheads and additional die cost. Digital-power-management blocks inherently require complicated physical power distribution and unavoidable gaps between the power islands. Isolation cells, level shifters, power-management signals, and other structures that relate to the power islands require smaller overheads. They might, however, cause issues in timing-critical or congested designs, increasing the risk to the program schedule.

IP selection is more complicated. You must ensure that you can integrate the IP into your IC using particular low-power techniques. With digital IP, for example, if you wish to use voltage scaling, then it is useful to know at what voltage-frequency pairs in the target technology the IP has been silicon proven. For analog IP, low-power standby modes or full voltage gating may require a redesign. You must pay for any required modification of the IP, increasing risk. Don't underestimate the amount of additional due diligence necessary for IP selection.

Access to voltage-scalable libraries may also increase IP-licensing costs. If your design requires multiple voltage levels, you must have access to more expensive voltage-scalable libraries. Multivoltage support is not yet widespread, however, reducing the number of potential library vendors and, hence, the ability to negotiate on price.

EDA tools supporting power islands

are also more expensive. Implementing power islands requires EDA tools to support simultaneous optimization in MMMCs (multiple modes/multiple corners). EDA licenses enabling these advanced and innovative features are expensive. On the other hand, without the automated-tool support, manual low-power tasks would become difficult, and risks would likely exceed acceptable levels.

You must also consider that EDA tools are still immature, leading to increased risk and increased NRE costs. Despite the fact that the tools have automated many tasks, they are still evolving. You will likely find issues with a tool implementation, and, if you are lucky, you will discover these issues before tape-out. Example issues may include incorrect placement of buffers from one domain within another domain, which could be independently powered off. Another issue arose in which buffers with antenna diodes were placed at the inputs to a power domain. In this case, turning off the power domain caused a large leakage current through the antenna diode from the on domain that was driving it.

In any case, detection of tool issues relies on designers' experience, a deep understanding of the intent, and good luck. It is natural that the tools take some time to mature, but you must consider their imperfections as risks having an impact on effort, time to market, and even the correctness of the design.

Remember that human mistakes and omissions are also likely. Although the EDA tools support system architecture, verification, and implementation, the most important design and data-management tasks require human intervention and experience. Because these issues become more complex when you use power islands, human mistakes and omissions constitute substantial risks.

Using power islands also increases postsilicon validation and production-test costs. Even after silicon returns, validation of multiple power modes requires increased NRE costs. Production tests may take more time and be more expensive due to the need for multivoltage testing to catch voltage-dependent bridging and delay faults.

Using power islands may incur an additional cost for training of technical staff. To produce competitive results and avoid expensive trial-and-error loops, your engineers may require training in design techniques for voltage islands or use of advanced tool features.

REDUCING OVERHEAD

Many strategies exist for reducing the overhead you incur when using power islands. First, consider your power strategy upfront. The best chance of achieving efficient power management for your design is at the architectural stage. Potential power savings dramatically decrease when you postpone decisions to later design phases (**Figure 3**). Some tools are available for the architectural phase of the design. Using a rough design specification, a list of required IP, technology models, and the like, they can help to partition your design into power domains, select voltage levels, select the most appropriate IP, specify details of the power intent, define functional modes, and select technology. The tools perform rapid what-if analysis and provide early estimations of power, floorplan, package, and die area. Using the results, the tools can then explore the cost benefits of low-power techniques.

You should consider the impact of power islands on all design tasks. Involve system architects, verification engineers, and implementation engineers in early design planning. Analyze tradeoffs between the power savings and associated verification, implementation, and area overheads as early as possible to build a robust and defensible schedule.

You should also adopt an approach that embraces the main standards for capturing power intent: CPF (Common Power Format) or UPF (Unified Power Format). Using these standards ensures that the power intent remains

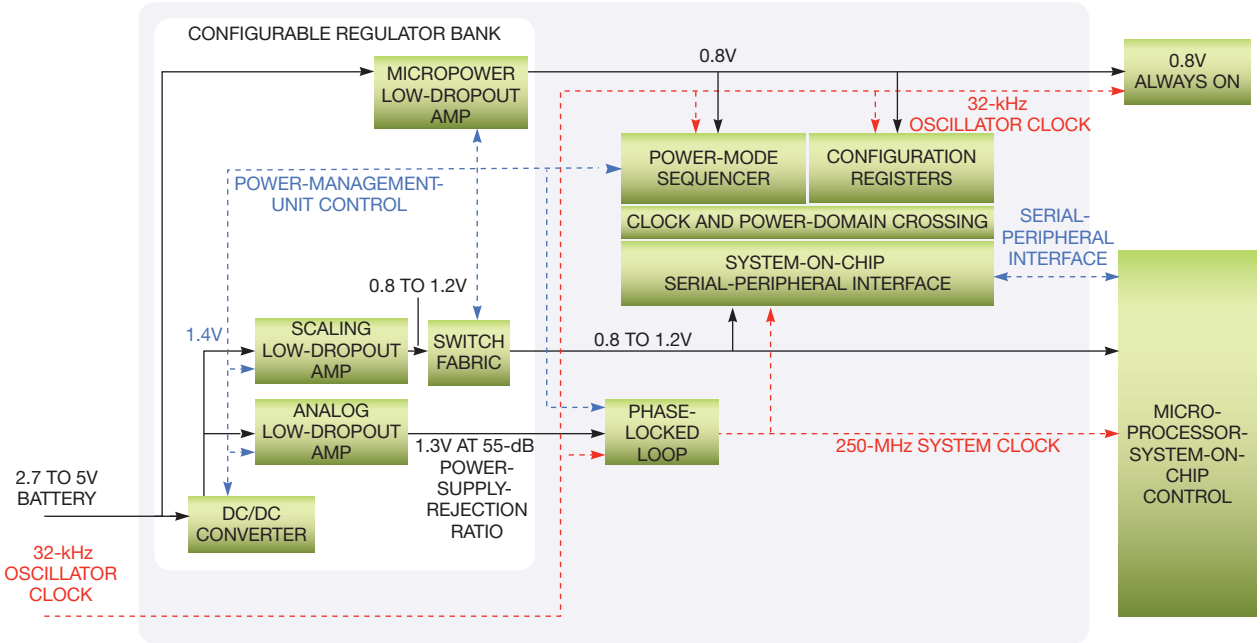

Figure 4 ICs with multiple power islands involve complex power-domain management and supply generation.

consistent throughout all design steps and is independent of the design data. Advanced EDA tools support CPF/UPF in all design phases. The tools can, for example, emulate and verify the power structures at RTL and their impact on the design's performance without a physical implementation. The tools then automatically insert the power structures into further design steps. CPF and UPF allow power-intent what-if analysis without modifying the verified RTL code. Without the CPF/UPF approach, implementing the power-saving techniques would be more complicated and require additional NRE costs. Hence, a CPF/UPF approach is a must.

Minimize the number of power domains your design requires. Currently, the most popular power-management method uses a single voltage supply with one always-on domain and one or two power-gated domains. This approach can massively reduce leakage power in idle modes and can reduce dynamic power by turning off the clock tree down to a root point. This type of partitioning is straightforward from an implementation point of view. Be aware that increasing the number of power islands can exponentially increase the implementation's complexity (**Figure 4**).

Try to minimize the impact of using multiple supply-rail-voltage levels. Multiple supply rails require more complex analog power sources and on-chip power routing. However, reducing the voltage from 1.2 to 1V, for example, can reduce the dynamic power by 44%, so the argument to add a rail can be compelling. If you add a supply rail, in volumes of more than 200,000 units, integrating a dc/dc converter or low-dropout regulator on the IC can reduce costs by amortization of additional NRE costs or IP-license fees in savings on the per-unit cost. Use of a low-dropout regulator without a capacitor instead of a normal linear regulator can reduce the number of I/O and external components you need if the source has to supply only a steady current without large fluctuations.

Consider minimizing the amount of dynamic-power adjustment your design will require. Having a static-power configuration at reset or just two major power modes significantly reduces the NRE costs. With more adaptive voltage scaling or combinations of powered-down islands comes the creation of more corner cases for architecture analysis, verification, static-timing analysis, and production test.

Use the best EDA tools available. Some EDA tools are more mature than others. Check how many designs with voltage islands that version of the tool has done, and check what the known issues are. S3 Group uses the NanoPower flow, which the company built on the EDA tools, to handle tool issues. Fixes then automatically apply to subsequent designs.

Finally, select partners that understand power islands and their implementation. Consider outsourcing parts of the design if power management is not your core competence. Apart from the experienced team with a real working knowledge of voltage islands, a design partner can also offer access to a wider range of required EDA tools. Engagement with a specialized partner can dramatically reduce elapsed time, risks, and the total cost of program execution.

To sum up, reducing power consumption is an imperative for most modern applications. Splitting the design into power islands is an effective technique for reducing power, particularly in deep-submicron technologies, and is therefore a common approach. Power islands inevitably increase the complexity of designs and result in higher costs, higher risks, and longer schedules. You cannot eliminate the overhead, but you can successfully manage or reduce them through careful planning, ensuring that engineering teams take advantage of the appropriate EDA tools and lessons that others have learned. EDN

AUTHORS' BIOGRAPHIES

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A MAGIC TOUCH: THE CONCEPT'S SOUND, BUT IMPLEMENTATION OPTIONS ABOUND

BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

Judging from the hype that Apple's promotional machine has turned out, some might think that the company single-handedly brought the touchscreen interface to market when it almost four years ago introduced the first-generation iPhone (**Figure 1**). *EDN* readers are too sophisticated for such marketing shenanigans, of course; some readers were likely developing touchscreen-based systems many years before Steve Jobs' Macworld Expo address in January 2007. Simplistically speaking, a touchscreen is nothing more than a semitransparent variant of a touch, or track, pad, an interface technology that dates back to a 1971 prototype. It saw initial Apple production successes in 2003's third-generation iPod and the 2004 PowerBook 500 series.

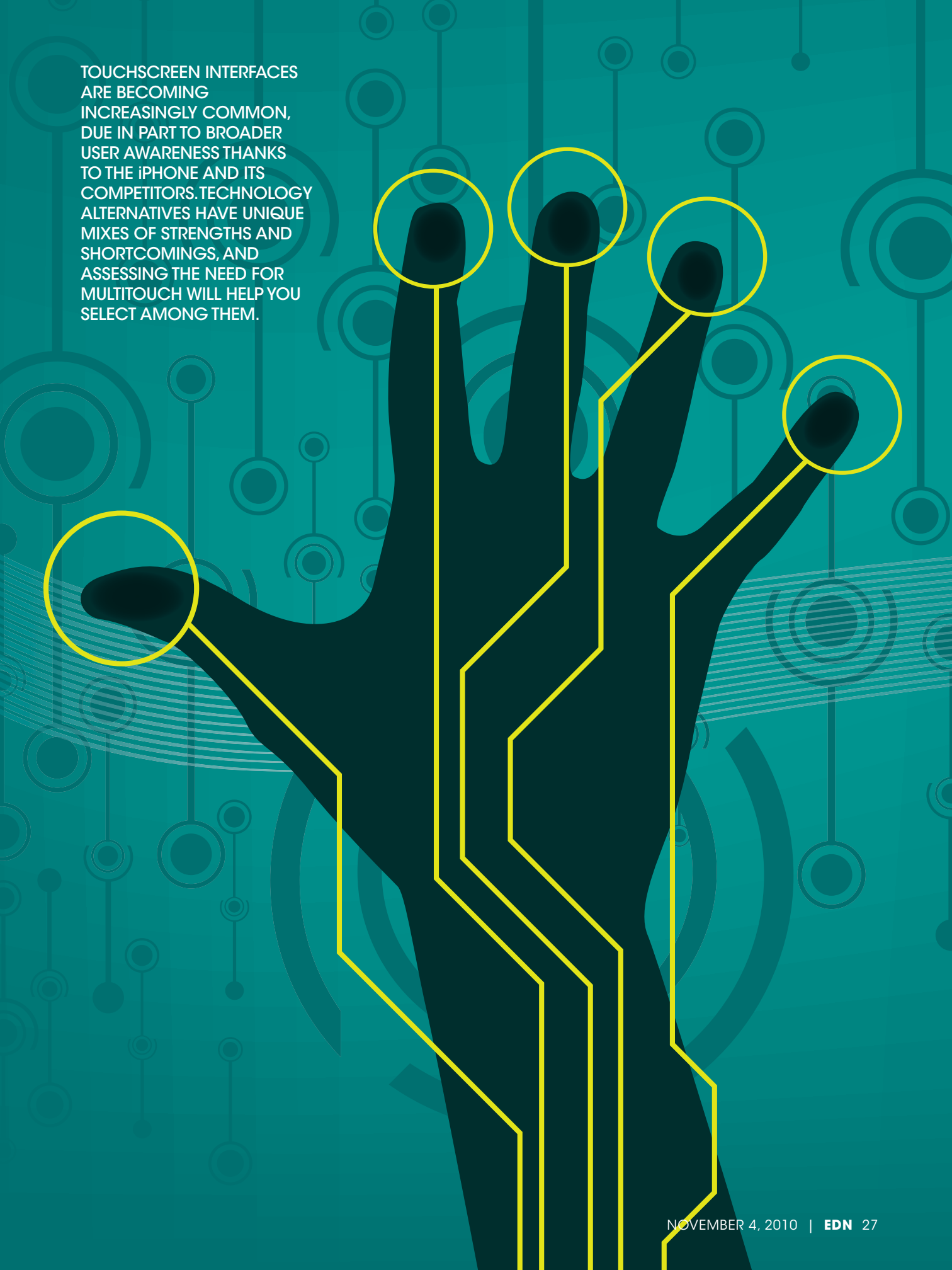
Most touch-interface patents hark back to the 1970s and 1980s—good news for those considering incorporating touchscreens into future designs because the patents' resultant expirations translate into broader touch-component sourcing and lower prices than might otherwise be the case. This article focuses on passive-touch technologies that leverage one finger or multiple fingers or an unpowered stylus; so-called active-touch systems employing light pens and the like are even more archaic but have largely fallen out of favor in recent years (see **sidebar** "Lesser-known touch creations also deserve your consideration").

Passive-touch technologies come in many varieties, and your imagination is the only limit on the resultant gesture implementations (**Reference 1**). However, some interface methods better match up than others with certain touch approaches. The environment in which your touch-augmented system will operate may also have a notable influence on which touch variant you select. Although display-disconnected touch pads remain popular, the touchscreen-enabled ability to directly link the visually sensed icons and other graphical elements to the tactile interface-manipulation function is a powerful and intuitive improvement for system users. Haptic vibrational feedback can further enhance the usage experience, and careful upfront technology selection will reap tangible dividends later.

RESISTIVE MATURATION

Companies such as Fujitsu Component Ltd vigorously promote the resistive touchscreen, which was the first touch-enhanced display approach to achieve widespread adoption. Today, resistive touchscreens remain the most widely adopted approach across all application segments, although upstart capacitive touchscreens are steadily superseding them, especially in consumer-electronics devices. Resistive touchscreens' fundamental attributes include low-cost hardware and a low-complexity system algorithm, which minimizes the required performance and power consumption of interface and control

TOUCHSCREEN INTERFACES ARE BECOMING INCREASINGLY COMMON, DUE IN PART TO BROADER USER AWARENESS THANKS TO THE iPHONE AND ITS COMPETITORS. TECHNOLOGY ALTERNATIVES HAVE UNIQUE MIXES OF STRENGTHS AND SHORTCOMINGS, AND ASSESSING THE NEED FOR MULTITOUCH WILL HELP YOU SELECT AMONG THEM.



circuitry. It's easy to grasp the elementary operation of a basic four-wire resistive touchscreen. It comprises a flexible outer membrane, whose resultant "soft" feel some users disapprove of, with a conductive coating typically comprising semitransparent ITO (indium-tin oxide) on its underside and a transparent glass or another substrate coated with conductive material on its topside (**Figure 2**).

Periodic insulating spacer "dots" reinforce an air gap between the membrane and the substrate. Pushing down on the outer membrane "short circuits" the two conductive layers at an intersection point, thereby defining the touch-placement location. According to Tyco Electronics' division Elo TouchSystems, the controller first applies 5V to the back layer. Upon touch, it probes the analog voltage with the cover sheet, reading 2.5V, for example, which represents a left/right position, or X axis. It then flips the process, applying 5V to the cover sheet, and probes from the back layer to calculate an up/down position, or Y axis. Only three—5V, ground, and probe—of the four wires are in use at any time (**Reference 2**).

Four-wire resistive touchscreens' simplicity also leads to one of the approach's biggest shortcomings: reliability. According to Elo TouchSystems' documentation, the primary drawback of four-wire technology is that one coordinate axis—usually, the Y axis—uses the outer layer, which is a flexible cover sheet, as a uniform voltage gradient. The constant flexing that occurs on the outer cover sheet with use eventually causes microscopic cracks in the ITO coating, changing its electrical resistance, thereby degrading the linearity and accuracy of this axis. The successor five-wire resistive touchscreen somewhat alleviates these issues at the trade-off of a somewhat higher BOM (bill-of-materials) cost. One wire goes to the cover sheet, E (**Figure 2d**), which serves as the voltage probe for X and Y. Four wires go to corners of the back glass layers, A, B, C, and D. The controller first applies 5V to corners A and B and grounds C and D, causing voltage to flow uniformly across the screen from the top to the bottom. Upon touch, it reads the Y voltage from the cover sheet at E. The controller then applies 5V to corners A and C and grounds B and D and again reads the X voltage from E. A five-wire touchscreen uses the stable bottom layer for both X- and Y-axis measurements. The flexible cover sheet acts only as a voltage-measuring probe, meaning that the touchscreen continues working properly even with nonuniformity in the cover sheet's conductive coating.

Resistive touchscreens can work with

AT A GLANCE

- Resistive touchscreens date from the mid-1970s and remain the dominant approach.
- Capacitive-touch displays deliver enhanced transparency and multitouch capabilities, but EMI (electromagnetic interference) and moisture sensitivities, along with other shortcomings, make them unpalatable for many applications.
- Pressure-sensitive touch sensors blend the attributes of traditional resistive and capacitive approaches, albeit for now only in "button-replacement" functions.
- Proximity sensing offers interesting additional near-touch capabilities.
- Other less-popular touch technologies may still be the right fit in your design.

Figure 1 Apple didn't really invent multitouch, as the company claimed when it unveiled the first-generation iPhone (a) in early 2007, but it and its successors broadened public awareness of the technology. The touch wheel first appeared in the April 2003 third-generation iPod Classic (b), in which it replaced its predecessors' buttons. Apple's first laptop with an integrated track pad, replacing precursors' trackballs, was the May 1994 PowerBook 500 Series (c). The company brought capacitive touch to input devices with the August 2005 Mighty Mouse (d), and Apple began just a few months ago selling the Magic Trackpad (e), which could potentially replace the mouse.

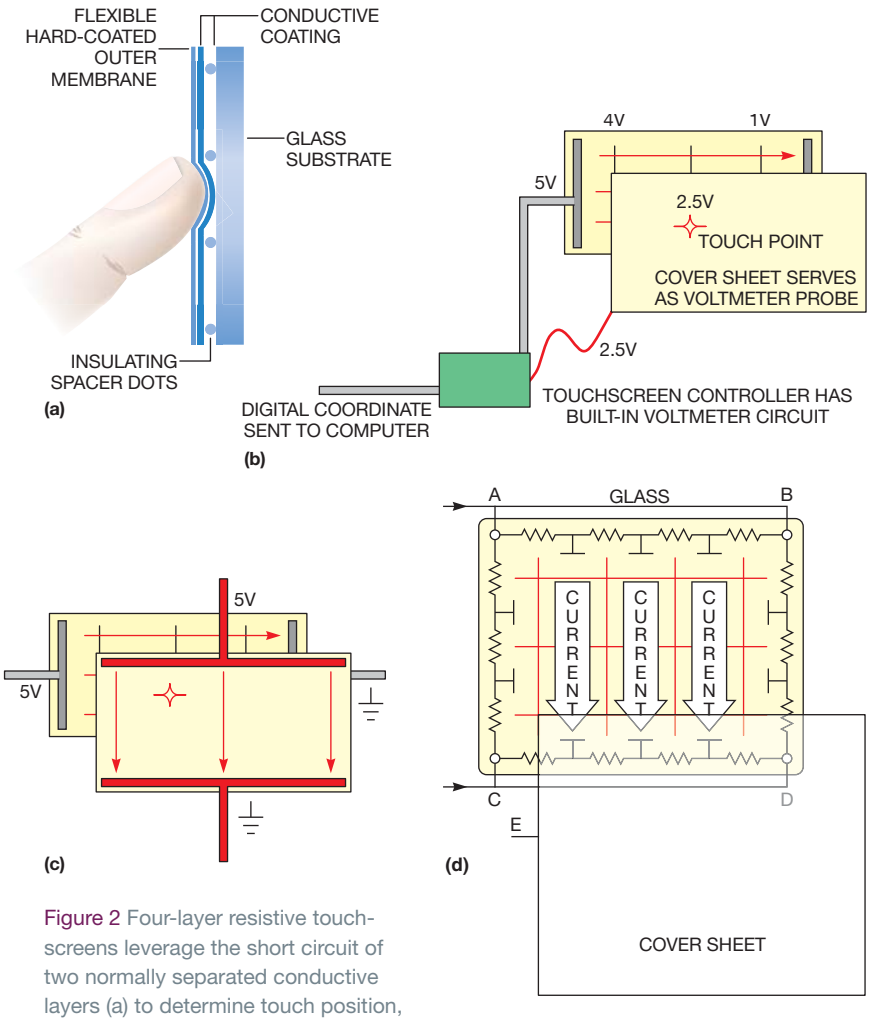


Figure 2 Four-layer resistive touchscreens leverage the short circuit of two normally separated conductive layers (a) to determine touch position, beginning with the X-axis location (b). Switching the high-voltage-and-ground application to the cover sheet and then probing from the back layer provides the Y-axis coordinate (c). A five-wire resistive implementation is somewhat more complex and costly but significantly improves reliability by leveraging the touchscreen only for probing purposes (d) (courtesy Elo TouchSystems).

any force-delivering input device, including a stylus, which is critical, for example, when entering Kanji and other complex-symbol characters; a credit-card edge; or a gloved finger. Conversely, any spurious pressure, such as cleaning the display with a cloth, causes unintended resistive-touchscreen activation. The devices are also inherently highly immune to EMI (electromagnetic interference) and moisture. Although the five-wire approach makes significant improvements in resultant durability and reliability, a not-unlimited number of touch activations still constrain the devices. The exact number of these activations before the devices fail depends on the stylus material's hardness, the tip point's severity, and the average user-applied touch pressure. Before a "hard" failure, a resistive touchscreen requires periodic user re-calibration to account for ITO degradation and membrane expansion and contraction in response to changes in ambient temperature and humidity.

TOUCH CONSUMERIZATION

The pressure-activated nature of a resistive touchscreen also makes it difficult both for a user to initiate a multitouch input and for system hardware and software to accurately decode it. This inherent limitation may at least in part explain why Apple went with an alternative capacitive touchscreen in the original iPhone, a design decision that the company has sustained with subsequent iPhone, iPad, and iPod touch iterations, as well as with the latest (sixth) generation of the iPod nano.

Apple wanted, for example, users to be able to zoom in or out a browser screen, map, or still or video image by moving two simultaneously applied finger tips toward or away from each other.

A touchscreen's light-transmission capability is also a critical consideration in a consumer-electronics device because it defines the required intensity of an LCD's (liquid-crystal display's) backlight or the user's perceived brightness of a self-illuminating OLED (organic-LED) display. It therefore also defines the system's BOM cost and the battery size and weight necessary to deliver a given amount of operating life between charges (**Figure 3**). The typical light transmission of a resistive touchscreen is 80% or less, whereas that of a capacitive touchscreen is often 90% or higher. As with resistive touchscreens, the use of ITO delivers the highest transparency of any possible cost-effective material for implementing capacitive sensors.

Capacitive touchscreens come in two fundamental varieties. Surface capacitance is the simplest approach, albeit the most limited from an application standpoint. The manufacturer conductively coats one side of a transparent insulator, such as glass; during normal system operation, a voltage applied to the conductive coating creates a uniform electrostatic field. The subsequent placement of a conductive touch-input device, such as a finger or a metal stylus, on the screen stimulates a change in capacitance. Measuring the capacitive change at various locations along the display's edges, such as in the corners, ascertains a rough estimate of location.

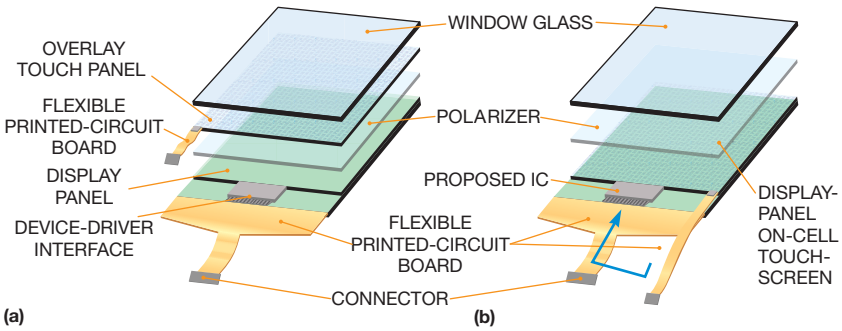


Figure 3 Samsung claims that a traditional touchscreen (a) is more complex and costly than the company's OLED approach (b).

Projected-capacitance touchscreens have a more complex construction but deliver more accurate location sensing as a result. They embed an etched XY single- or dual-perpendicular-layer conductive grid within the transparent insulator (**Figure 4**). Projected capacitance comes in two variations. In mutual capacitance, the touch input changes the mutual capacitive coupling between sequentially scanned row and column electrodes, with a capacitor at each etched row/column junc-

LESSER-KNOWN TOUCH CREATIONS ALSO DESERVE YOUR CONSIDERATION

Resistive- and capacitive-touchscreen technologies are on-cell approaches because the sensors lie in layers above the LCD's (liquid-crystal display's) or OLED (organic-LED) display's pixels. Alternatively, it's possible to construct an in-cell touchscreen in which, alongside the pixel circuitry, the manufacturer places a photodiode or another light-sensitive circuit, voltage-based microswitch, or charge-sensing capacitive element or another electrode.

More generally, as Wikipedia's entry for "touchscreen" points out, several other technologies are vying for your attention. These approaches include SAW (surface acoustic wave), infrared, strain gauge, optical imaging, dispersive signal, and acoustic pulse recognition. Each of these approaches comes with a corresponding set of strengths and shortcomings (Reference A). According to the Wikipedia entry, SAW technology uses ultrasonic waves that pass over the touchscreen panel. When a user touches the panel, it absorbs a portion of the wave. This change in the ultrasonic waves registers the position of the touch event and sends this information to the controller for processing.

An infrared touchscreen uses an array of infrared XY LED and photodetector pairs around the edges of the screen to detect a disruption in the pattern of LED beams, whereas, in strain-gauge, or force-panel, technology, the screen is spring-mounted on the four corners, and strain gauges determine deflection when a user touches the screen. In optical imaging, two or more image sensors lie around the edges—mostly in the corners—of the screen. Infrared backlights in the camera's field of view reside on the other side of the screen. A touch shows up as a shadow, and each pair of cameras can be triangulated to locate the touch or even measure the size of the touching object (see sidebar "Microsoft Surface: touch technology everyplace or a focus misplaced?").

Another approach, dispersive-signal technology, uses sensors to detect the mechanical energy in the glass that occurs due to a touch. Complex algorithms then interpret this information and provide the actual location of the touch. In contrast, acoustic pulse recognition uses piezoelectric transducers at various positions around the screen to turn the mechanical energy of a touch into an electronic signal. The screen hardware then uses an algorithm to determine the location of the touch based on the transducer signals.

You should research these approaches, for example, if your application has atypically large touchscreen dimensions or nontraditional operating-environment requirements.

REFERENCE

A "Touchscreen," Wikipedia, http://bit.ly/cTBZSv.

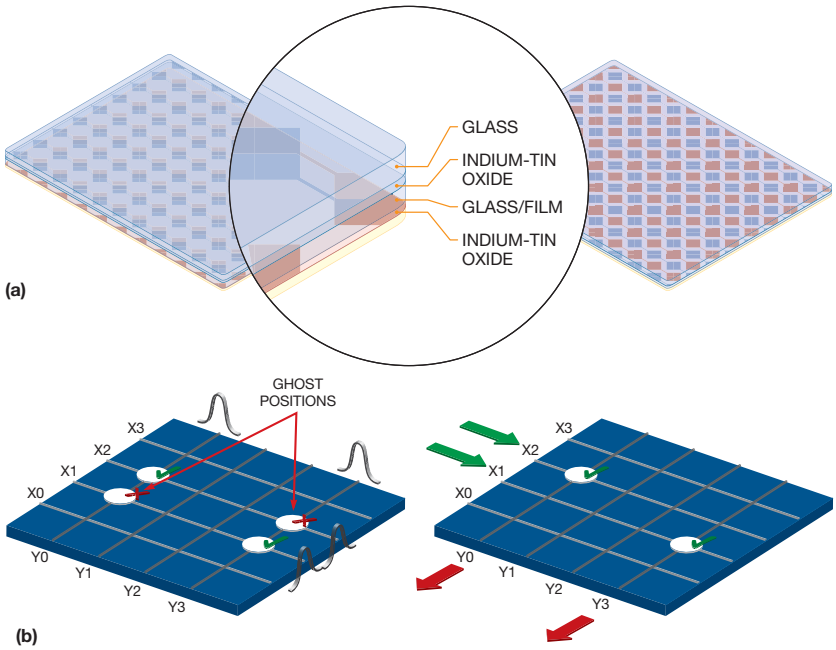


Figure 4 Projected-capacitance touchscreens enable more accurate location discernment than their simpler surface-capacitance counterparts (a, courtesy Cypress Semiconductor). The mutual-capacitance implementation suffers no "ghosting" inaccuracy of its self-capacitance alternative in multitouch applications (b, courtesy Atmel).

tion. With self-, or absolute-, capacitive-touch technology, conversely, the touch input alters the sensor's parasitic capacitance to ground. Self-capacitance systems deliver higher sensed-signal strength than their mutual-capacitance counterparts, but they cannot accurately resolve more than one simultaneous input in all possible cases because two fingers on one grid line deliver the same result as one. Self-capacitance systems are also prone to wrong-location "ghosting" errors (see **sidebar** "Multitouch technology: truly necessary?"). Mutual-capacitance systems are conversely the optimum approach for true multitouch designs. These systems sequentially voltage-pulse each X line and scan Y lines for capacitance changes. The mutual-capacitance system's touchscreen

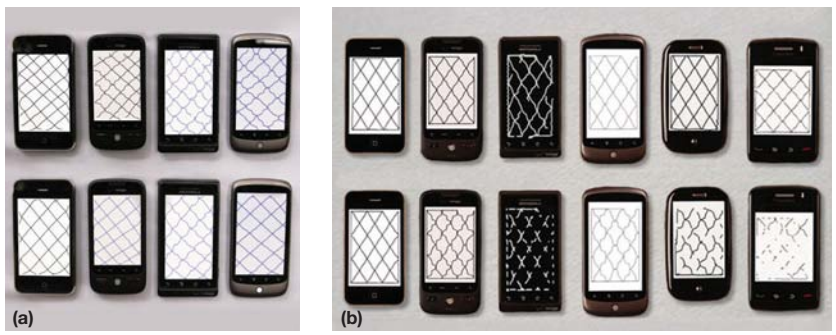


Figure 5 Moto Development Group's testing (a) of (from left) Apple's iPhone, HTC's Droid Eris, Motorola's first-generation Droid, and the HTC-designed Google Nexus One revealed wide variance in accuracy both among handsets from different manufacturers and among those from the same manufacturer. These variations appear in situations with light pressure using the corner of a finger pad (top row) and medium pressure using a full finger (bottom). Follow-on testing (b) using more precise robotic-controlled input patterns included the same four models from left to right, plus the Palm Pre (second from right) and the Blackberry Storm (right). These tests used a 7-mm robotic finger for a medium touch (top row) and a 4-mm robotic finger for a very light touch (bottom).

MICROSOFT SURFACE: TOUCH TECHNOLOGY EVERYPLACE OR A FOCUS MISPLACED?

One of the more baffling research projects to receive production approval from Microsoft's executive staff in recent years is Surface, a 30-in. touch-table technology that the company publicly unveiled in May 2007 (Figure A). Its initial customer was AT&T, which began installing Surface equipment in retail stores 11 months later. Some casinos, hotels, restaurants, and retail outlets also use Surface, and several news and television programs have showcased it. Nonetheless, it has enjoyed a muted market embrace at best, and Microsoft has released little Surface news since March 2009, when the company reported that it was working with 120 application-developing partners in 11 countries.

Figure A Microsoft's Surface very-large-touchscreen technology has achieved limited success in some casinos, restaurants, hotels, and retail outlets, but a mass-market embrace has so far eluded it.

Questionable success aside, Surface is an impressive technical achievement and an example of optical-imaging-touchscreen technology. Underneath the reflective surface is a 1024×768-pixel XGA (extended-graphics-array)-resolution DLP (digital-light-processing) projector, along with an infrared projector that shines upward to bathe the table with invisible light. Five cameras within the Surface housing redundantly detect infrared-light reflections from objects resting on and near the tabletop, delivering a 360° field of view. However, the reliance on infrared-light detection precludes Surface's use in, for example, direct-sunlight environments.

Surface can respond to as many as 52 simultaneous touches. It can recognize objects, including fingertips and bar codes, and gestures, and it can track motion. The current commercial version of the Surface hardware runs a custom variant of the Windows Vista OS and uses a custom system board roughly the size of two conventional ATX motherboards with a 2.13-GHz Intel Core 2 Duo CPU, 2 Gbytes of DDR2 SDRAM, a 250-Gbyte SATA hard-disk drive, 10/100-Mbps wired Ethernet, IEEE 802.11b/g Wi-Fi, and Bluetooth v2.0 wireless connectivity.

controller individually addresses each XY-intersection node, and the system uniquely senses all touch points.

Capacitive touchscreens also tend to be more durable than their resistive predecessors because input pressure doesn't deform the conductive material, and they are immune to unintended pressure-based input effects, such as from cleaning cloths. However, this advantage is true only if you use a dry, static-free cloth. Any environmental factor, including EMI and water, that can alter a display's surface capacitance is a potential candidate for a capacitive touchscreen's operational error. Conversely, any environmental factor that inhibits an input device's usual capacitance-altering behavior, such as a glove on a hand or a nonconductive coating on a stylus, also results in unintended capacitive-touchscreen responses or lack thereof. And, as a recent experience with a capacitive touchpad highlights, a capacitive touchscreen's behavior depends greatly on the quality of the power supply feeding it (**references 3** and **4**).

Capacitive-touchscreen systems tend to be far more algorithmically intensive than their resistive-touch counterparts, translating into more elaborate software routines that demand faster and, therefore, more power-hungry processors to guarantee a given response time to user input. A design engineer might attack this issue by "freezing" portions of the algorithm into lower-power hardware gates rather than relying exclusively on software subroutines. However, the capacitive-touchscreen market is relatively immature, so easy system upgrades to fix bugs and add enhancements are desirable during design, on the production line, and in users' hands. This need for straightforward upgrades for now generally precludes such a silicon-translating step. Representing the diversity of capacitive-touchscreen implementations currently vying for customers' design wins, industry-research company Moto Development Group, which Cisco Systems subsequently acquired, has performed laboratory analysis that revealed radically varying across-screen accuracy patterns for popular smartphones, even with precise robot-powered input touch patterns (**Figure 5**).

PRESSURE, PROXIMITY

Although cutting prices might temporarily secure a semiconductor supplier a few design wins, a unique and equally important, customer-valued set of features is a more reliable means of securing sustained market success. This strategy is clearly evident in the approaches that touch-controller vendors including Cypress Semiconductor and Microchip Technology have taken. Microchip blends the attributes of traditional resistive- and capacitive-touch technologies, which it brands with the mTouch marketing moniker (**Figure 6**).

Several years ago, Microchip unveiled an inductive approach whose "fundamental operating principles enable it to work through a front panel, such as plastic, stainless steel, or aluminum," according to the company. "The technology also works through gloves and on surfaces that contain liquids" (**Reference 5**). More recently, Microchip broadened mTouch to encompass a different capacitive approach, albeit with a similar outcome. In the company's initial mTouch inductive technique, an inductive coiled sensor senses a flexible front panel with an approximately 10-micron deflection. An elec-

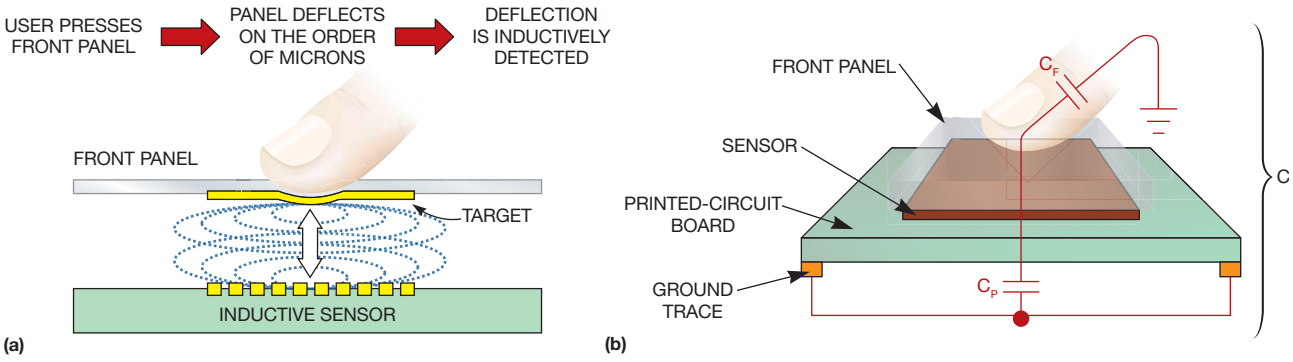


Figure 6 Nonconductive input sources, such as gloved hands, can use pressure to operate Microchip Technology's mTouch. The company augmented its initial 2008 inductive approach (a) using a capacitive technique (b).

trically or magnetically conductive target resides on the panel's opposite side. The sensor reports the input to an ADC, typically residing within an embedded microcontroller.

The more recent capacitive mTouch technique again relies on slight depression of a front panel relative to a sensor below it. This time, though, the panel-plus-sensor combination implements a two-parallel-plate capacitor. The matched controller IC detects the touch-induced change in capacitance, the result of bringing the two plates closer together. Microchip is now focusing mTouch on mechanical-button, toggle-switch, and dimmer-replacement opportunities, but it will also be conceptually applicable to multisensory-touchscreen applications in the future.

Cypress, by boosting the discerned SNR (signal-to-noise ratio) of its CapSense technology, claims that it can now discern not only a finger resting on a panel but also the slight capacitance change caused by a finger that's close to but hasn't yet made contact with the sensor-inclusive assemblage. Again, the company's current focus is on elementary button- and switch-replacement designs, with more elaborate touchscreen opportunities on the long-term horizon. The potential applications are interest-

MULTITOUCH TECHNOLOGY: TRULY NECESSARY?

Your decision on whether to select projected capacitance-touchscreen technology, specifically the mutual capacitance variant of it, hinges in part on whether your application requires the ability to simultaneously decode the location and movement direction and rate of two or more touch inputs. You might believe, for example, that the zoom, sweep, and rotate capabilities of modern high-end cell phones and track pads indicate that they implement multitouch support.

However, a recently published article by Larry Mozdzyn, chief technology officer of Ocular Inc, disagrees (Reference A). "Despite what you may read in articles or hear in advertisements, typical gesturing on most smartphones is not a true multitouch implementation," the article notes. The touch controller for a gesture interprets only relative movements of one or two touches on the panel and reports these movements as predefined gestures. For example, the "pinch" gesture, in which the thumb and forefinger move together to resize a window, seems to imply a true multitouch event, the article states, but the controller recognizes only the movement of those touches relative to each other. If the relative touch movements fit the predefined characteristics of a pinch, then the controller will report a pinch. In true multitouch, the controller will provide a detailed report of data such as touch location, area, angle, and other features. The simple "gesture-only" touch controllers do not have the level of sophistication and processing power to provide these enhanced functions, the article concludes.

However, there's a contrarian view: The more elaborate the touchscreen interface, the more demanding the system specifications that are necessary to support it and the more limited the list of touchscreen-technology candidates that can implement it. Simplify your touch approach, and you'll likely also simplify your sourcing strategy and positively affect system cost, power consumption, and other important variables. If users will accept elementary multifinger gestures, why would you bother pursuing a more sophisticated implementation path? Even multi-input gesture-only capabilities may be overkill; consider the Google Android operating-system case study, for example. Android variants that emerged before Version 2.0 supported only single-finger inputs. Google handled zoom-in and -out functions, for example, by displaying magnifying glass plus and minus icons that a user would repeatedly tap—not the ideal scenario but a functional one. A single-finger input also suffices for moving around within an image or application screen and for sweeping between images and screens.

REFERENCE

A Mozdzyn, Larry, "The True Meaning of Multitouch," *Design Talk*, Aug 31, 2010, http://bit.ly/bUFPIR.

ing to consider; the sensor could use an approaching finger as a sign to bring a display or even an entire system out of sleep mode. And, addressing Apple's concerns about Adobe Flash's supposed inability to support "mouse-over" capabilities with mouseless systems, a moving close-proximity finger could control an on-screen cursor, with the actual fingertip press on the panel signifying a mouse click.

Atmel, at least for the moment, seems content to focus on more traditional touch applications. The company's Web site reveals a focus on supporting ever-larger touchscreen-real-estate dimensions, along with ongoing improvements in response time, power consumption, and development-tool-suite ease of use and robustness. As for Synaptics, a name familiar to anyone who has designed track-pad-based systems, the company has broadened its product suite to include not only touchscreen controllers but also touchscreens themselves. All four controller suppliers tout their products' abilities to discern and ignore common touch-usage scenarios for which a response would be inappropriate, such as resting a palm on a tablet computer while typing on the virtual keyboard or gripping the powered-on tablet to pick it up or transport it. EDN

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Fujitsu Component Ltd www.fcl.fujitsu.com	**Tyco Electronics** www.elotouch.com

REFERENCES

1 Cravotta, Robert, "Recognizing gestures: interface design beyond point and click," *EDN*, Aug 16, 2007, pg 44, http://bit.ly/9gTHuL.

2 "Compare All Resistive Touch Technologies (4-, 5-, 6-, 7-, and 8-Wire Explained)," Tyco Electronics, http://bit.ly/cIO9vX.

3 Dipert, Brian, "Apple's MacBook Air: Above the ground, without a ground, the track pad goes down," *EDN*, July 9, 2009, http://bit.ly/aaFmno.

4 Dipert, Brian, "Track-pad troubles: a no-ground work-around," *EDN*, July 14, 2009, http://bit.ly/b76a9S.

5 "Microchip Technology Introduces mTouch Inductive Touch-Sensing Solutions," Microchip Technology, Nov 11, 2008, http://bit.ly/cP06K4.

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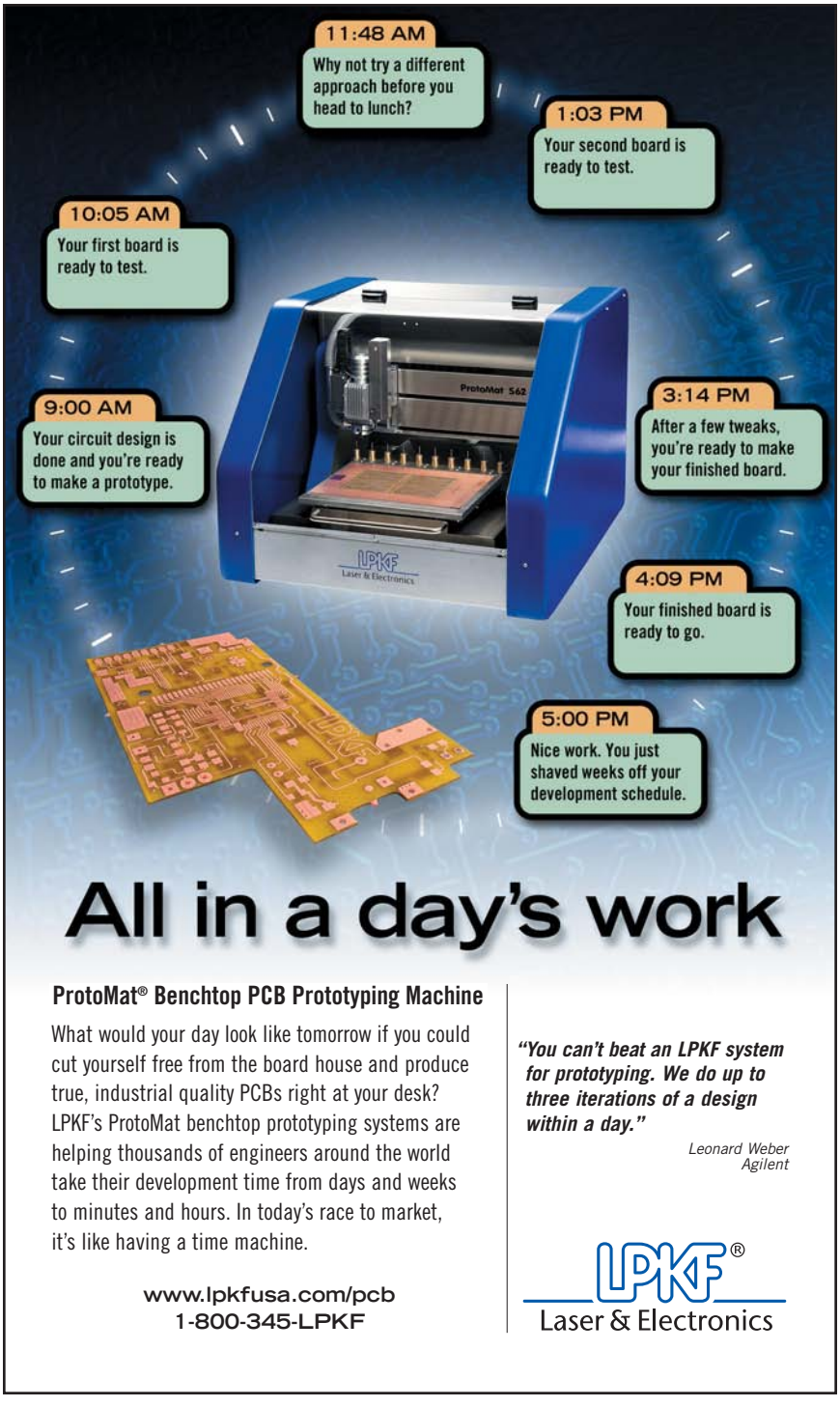

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Essential principles for practical analog BIST

PRACTICAL ANALOG BIST HAS THE POTENTIAL TO REDUCE IC-TEST COSTS AND TIME TO MARKET.

For almost 20 years, researchers and semiconductor manufacturers have been trying to develop a practical analog BIST (built-in self-test) for mixed-signal ICs. By enabling mixed-signal IC testing on digital testers and simpler multisite testing, this technique potentially reduces IC-test costs and time to market. Other anticipated benefits include faster test development and in-system self-test.

Most IC-design engineers understand the operation principles of digital BIST. It generates pseudorandom bit patterns with an LFSR (linear-feedback shift register) and applies them to a circuit under test using the flip-flops configured temporarily into serial shift registers. Digital BIST also captures responses using the same flip-flops, compresses the shifted-out result into a digital signature, and then bitwise-compares it to a correct signature. Although the details of industrial-logic BIST are more complex, the basic principles still apply for accommodating multiple clock domains, multicycle delay paths, and power-rail noise, for example.

The principles of analog BIST, however, remain enigmas to most engineers, especially analog-circuit designers. This fact became evident at the 2009 Design Automation Conference when an experienced PLL (phase-locked-loop)-circuit designer asked, "If your BIST for PLLs is so accurate, why don't you design PLLs?" To answer that question, you must first understand the principles of practical analog BIST.

HOW DO YOU DEFINE "ANALOG"?

An "analog" circuit means different things to different people. You can consider a PLL or a SERDES (serializer/deserializer) to be digital-, analog-, or mixed-signal. BIST tests for these units can be purely digital because these functions have only digital inputs and outputs. For example, some ICs measure their PLL's output frequency with an on-chip frequency counter—which counts the number of oscillation cycles in a known number of cycles of a reference frequency—that fails the test if any bit in the count differs from what you expect. Many ICs test their SERDES transceiver's performance by looping back pseudorandom data and failing it if it detects a bit error. However, testing analog circuits, such as ADCs or DACs, clearly requires BIST circuitry that can generate or capture analog signals—signals whose instantaneous voltage is always relevant. Traditional analog circuits, such as filters and linear voltage regulators, have analog inputs and outputs, although many have digital-control signals or clocks. The purest analog circuits, such as RF circuits, may have no digital aspects at all.

In testing, an analog circuit has at least one signal whose instantaneous voltage is nondeterministic. Testing comprises checking that the signal, which might be a digital word, is between two voltages, digital values, or time thresholds; that a signal statistic is between limits; or that a mathematical computation involving the signal produces a value between limits. You should apply analog-test principles to all circuits that have any analog signals.

Responses from purely digital circuits are deterministic, so an acceptable output signal is one that you need to sample only once. If you look at digital-circuit signals in enough detail, such as millivolts or picoseconds, however, every circuit is analog. This consideration is nontrivial for nanometer CMOS processes in which power-rail noise, jitter, temperature, and parametric variations are significant effects relative to 1V power rails and subnanosecond clock periods. BIST circuitry that tests analog is subject to these effects, even if the BIST is almost entirely digital, which is the reason that many analog designers wonder how any analog BIST can be more accurate than an analog circuit under test on the same chip.

THE CHALLENGE OF DESIGNING ANALOG BIST

Designing BIST for analog circuits involves more than accurately delivering and capturing analog signals. The variety of signals and parameters requiring testing is much larger than that of the logic zeros and ones that digital BIST handles. Analog stimuli and responses can range from dc voltages, linear ramps, and impulses to sine waves and frequency modulation. To complicate the challenge, the stimulus and response might belong to different domains. For example, a dc voltage input might generate a frequency output. The parameters requiring analysis further add to the challenge because they may range from amplitude, phase delay, and SNR (signal-to-noise ratio) to dc voltage, peak-to-peak jitter, and duty cycle.

Test equipment usually must be an order of magnitude more accurate than the circuit under test. So the most daunting challenge for analog BIST is how to economically achieve greater accuracy than the circuit under test, which presumably has achieved the best possible accuracy for its silicon area and technology. The range of signal amplitudes can be enormous. ADCs and DACs handle on-chip analog signals with dynamic ranges as high as 2^{24}, equivalent to eight orders of magnitude.

You can compare digital BIST to a student who is grading his own multiple-choice test. The student places a template

New Smaller and Faster Optical Isolation Amplifiers Feature 0.5% Gain Accuracy and 1140 Vpeak Working Voltage

Introduction

Many analog designers are familiar with differential instrumentation amplifiers but these will not provide the insulation voltages to withstand high transient voltages safely, nor the isolation to protect sensitive low voltage control electronics from high voltage switching circuits found in power conversion applications. With a -40° to 105°C operating temperature range, Avago's miniature ACPL-C79x Precision Isolation Amplifiers target industrial automation and instrumentation, renewable energy, and HVAC markets.

Based on Avago's proprietary optical isolation technology, sigma-delta analog-to-digital converters and chopper stabilized amplifiers, the ACPL-C79x isolation amplifiers are used for motor phase and rail current sensing, servo motor drive, switching power supply feedback isolation, DC link voltage monitoring, inverter current sensing and switching power supply feedback isolation. The ACPL-C79x high common-mode transient immunity of 15 kV/µs provides the ruggedness and stability needed to accurately monitor current in high-noise motor control environments.

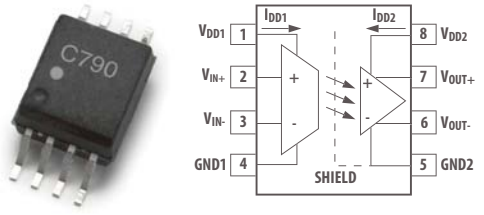


Figure 1. ACPL-C79X Package

As shown in Figure 1, the isolation amplifiers are fully differential, input and output, with a gain accuracy of ±0.5% (ACPL-C79B), ±1% (ACPL-C79A), and ±3% (ACPL-C790). Operating from a single 5 V supply, the isolation amplifier series features an excellent nonlinearity of 0.05% and a SNR of 60 dB. With a 200 kHz bandwidth and 1.6 µs response time, the ACPL-C79x captures transients during short circuit and overload conditions. The stretched SO-8 package has a footprint 30% smaller than the standard DIP-8 package. When mounted on a PCB, it occupies a space that is a fraction of that for a Hall Effect or transformer based isolation amplifier.

Key ACPL-C79x Key Features

- Fully Differential Isolation Amplifier
- ±0.5% High Gain Accuracy (ACPL-C79B)
- –50 ppm/°C Low Gain Drift
- 0.6 mV Input Offset Voltage
- Excellent 0.05% Linearity
- 60 dB SNR
- 200 kHz Wide Bandwidth
- 3 V to 5.5 V Wide Supply Range for Output Side
- -40°C to +105°C Operating Temperature Range
- Advanced Sigma-Delta (Σ-Δ) A/D Converter Technology
- 15 kV/µs Common-Mode Transient Immunity
- Safety and Regulatory Approvals (pending):
  - IEC/EN/DIN EN 60747-5-5: 1140 Vpeak working insulation voltage
  - UL 1577: 5000 Vrms/1min double protection rating
  - CSA: Component Acceptance Notice #5

Motor Drive Application Example

In a typical motor drive application, shown in Figure 2, currents through a small value current sense resistor cause a voltage drop that is sensed by the ACPL-C79x and a differential output voltage, proportional to the current, is created on the output side of the isolation barrier. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple three terminal voltage regulator (U1). The voltage from the current sensing resistor, or shunt (RSENSE), is applied to the input of the ACPL-79x through an RC anti-aliasing filter (R5 and C3). And finally, the differential output of the isolation amplifier is converted to a ground referenced single-ended output voltage with a simple differential amplifier circuit (U3).

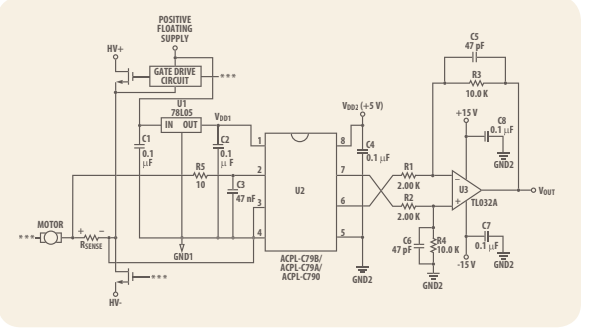


Figure 2. Typical motor current sense circuit

Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

Shunt Resistor Selection

A real-world motor current sense resistor calculation will show what must be considered in selecting the current sense resistor. First determine how much current the resistor will be sensing. The graph in Figure 3 shows the RMS current in each phase of a three phase induction motor as a function of average motor output horsepower and motor drive supply voltage. The maximum value of the sense resistor is determined by the current being measured and the maximum recommended input voltage of the isolation amplifier. For example, if a motor has a maximum RMS current of 10 A and can experience up to 50% overloads during normal operation, then the peak current is 21.1 A (=10 x 1.414 x 1.5). With a maximum amplifier input voltage of 200 mV, the maximum sense resistance would be about 10 mΩ. The maximum average power dissipation in the sense resistor, which is about 1 W in this example, should also be checked by multiplying the sense resistance times the square of the maximum RMS current. If the power dissipation is excessive, a lower resistance value can be used.

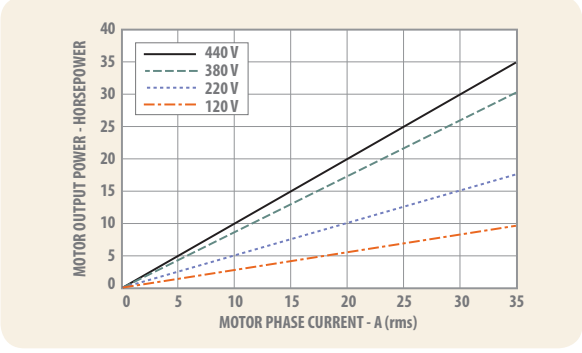


Figure 3. Horsepower vs. motor phase current/voltage

Differential Input Connection

In Figure 2, the isolation amplifier is connected in a single-ended input mode. However, given the fully differential input structure, a differential input connection, shown in Figure 4, can be used for better performance. Any noise induced on one pin will be coupled to the other pin by the capacitor C and creates only common mode noise which is rejected by the ACPL-C79x.

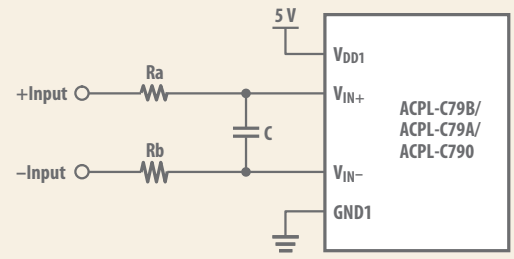


Figure 4. ACPL-C79x differential input connection

Voltage Sensing

The ACPL-C79B/C79A/C790 can also be used to isolate signals with amplitudes larger than its recommended input range with the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 kΩ) so that the input resistance (22 kΩ) and input bias current (0.1 μA) do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the 10 Ω series damping resistor is not (the resistance of the voltage divider provides the same function). The low-pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth.

Evaluate the ACPL-C79X

The ACPL-C79X evaluation board demonstrates the high linearity and low-offset capability of the ACPL-C79B/C79A/C790. It allows a designer to easily test the performance of the isolation amplifier in an actual application under real-life operating conditions. A surface mount shunt resistor is provided along with the board.

Figure 5. ACPL-C79x evaluation board

Summary

Avago's three new Miniature Precision Isolation Amplifiers, made possible by proprietary optical isolation technology, offer increased accuracy, speed, bandwidth and insulation ratings. Additional information is available at www.avagotech.com

over the answer sheet and counts the number of correct answers. Analog BIST, on the other hand, compares with a student who is grading his own essay answers. It's not a simple, objective procedure. Now that you understand the magnitude of the challenge, consider the fundamental circuit principles that you must apply for analog BIST to be practical.

FUNDAMENTAL CIRCUIT PRINCIPLES

The first principle is that the test mechanism itself must be testable by applying timing-insensitive digital-test patterns, clocks, and dc voltages without requiring off-chip linear ac signals or measurements. ATE (automatic-test equipment) undergoes extensive calibration and testing before it leaves the factory. For BIST to be an alternative to using mixed-signal ATE, you must calibrate and test it before using it. The purely digital portions of analog-BIST circuitry should be testable using scan-based tests, including logic BIST. If the digital circuitry includes delay lines or delay-matched circuitry, then you should test the delays and delay increments. You can measure a delay by including or configuring the delay line into a ring oscillator and measuring the oscillation frequency using an on-chip frequency counter.

Testing a purely analog portion of analog BIST is more complex. Some researchers have proposed using an ADC or a DAC in their analog BIST, implicitly assuming that ATE can test it first; however, mixed-signal ATE would still be necessary, thus eliminating many benefits of BIST.

Perhaps the oldest BIST technique is to loop back a DAC output to an ADC input or a modulator output to a demodulator input to permit an entirely digital test. This approach is analogous to using an untested circuit to test another and is insensitive to compensatory faults. For example, the DAC might have excessive nonlinearity for which similar nonlinearity in the ADC compensates, making the two together look better than either one alone.

The second principle of analog BIST is undersampling—sampling slower than the Nyquist rate, which means slower than twice the highest frequency of interest—which is necessary to permit slower analysis of a signal. Slower sampling also facilitates making the BIST circuitry smaller than the circuit under test.

In some self-calibration schemes, a low-speed ADC undersamples a high-speed ADC or DAC analog signal. First-order sigma-delta modulators are small, simple analog circuits that can convert analog signals into digital bit streams with arbitrary resolution if bandwidth decreases. A modulator might sample a signal 16 million times/second to produce 16 million 1-bit samples; the modulator can digitally filter these samples to produce 1 million 4-bit resolution samples/second or 16,000 16-bit samples/second, in each case decreasing the usable bandwidth by a factor of 16.

Undersampling permits a narrower bandwidth of interest to center on the original signal's frequency and allows its translation to a low frequency, at which it is easier to analyze. However, undersampling involves a trade-off of aliasing effects, which you must consider.

Another example of sampling is a PLL BIST that uses the PLL's input-reference-clock edges to sample the PLL's output (**Figure 1a**). In this case, a reference clocks a latch through an adjustable delay line, and the latch performs the sampling. The latch's output counts for, say, 1000 clock cycles, and then the delay is incremented. This action repeats until the latch obtains the cumulative distribution function (**Figure 1b**). The PLL's output frequency could be many times higher than its reference frequency. This BIST cannot detect jitter between reference-clock edges, but another technique that uses a slightly offset sampling frequency can sample at all points in the output phase (**Figure 2**).

These two techniques show an important principle of time measurement: Controlling the time at which a signal is sampled requires either a constant time offset from an adjustable delay or a constant frequency offset from an adjustable oscillator, such

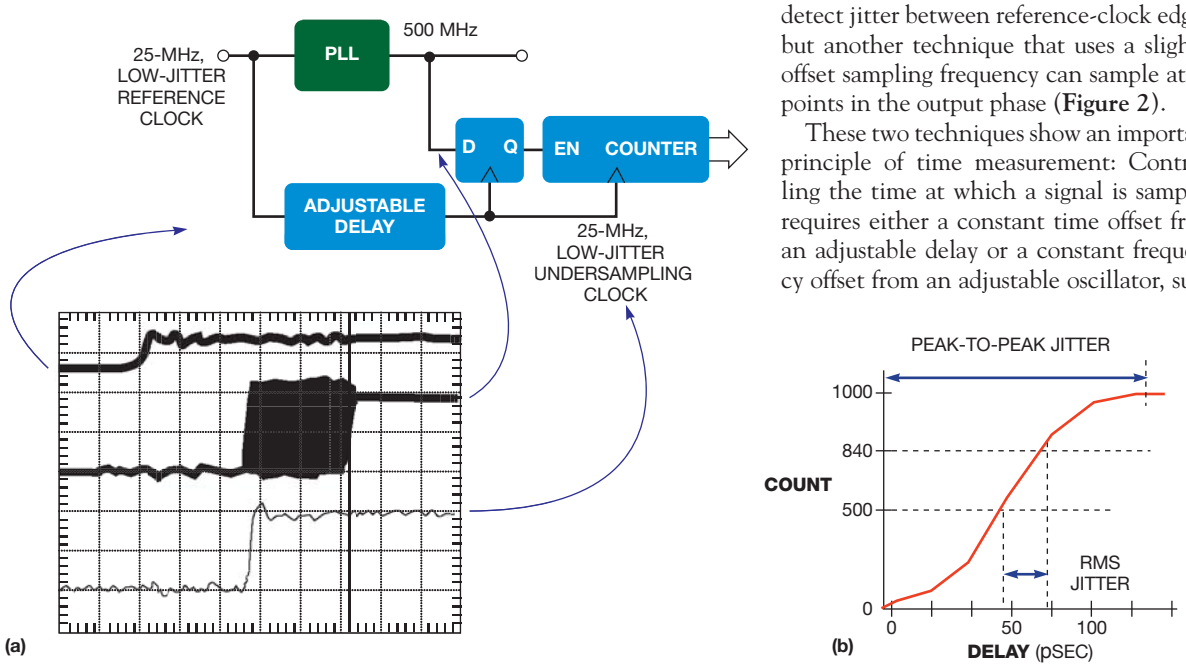


Figure 1 A PLL BIST uses the PLL's input-reference-clock edges to sample the PLL's output (a). A reference clocks a latch through an adjustable delay line, and the latch performs the sampling. The latch's output counts for, say, 1000 clock cycles, and then the delay increments. This action repeats until the latch obtains the cumulative distribution function (b).

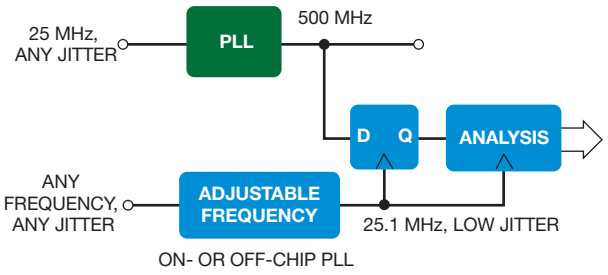


Figure 2 This BIST uses a slightly offset sampling frequency and can sample at all points in the output phase.

as a PLL. Low-jitter delays are increasingly more difficult to achieve in nanometer CMOS, but low-jitter frequency offsets are increasingly easier to achieve.

Another principle of analog BIST is subtracting systemic errors to improve accuracy. When measuring voltages, for example, you must cancel the offset voltage of any comparator or operational amplifier. If these circuits have negligible offset, then you must measure the offset to verify that it is negligible; otherwise, you must subtract its value. It is simpler to assume that the offset is significant and subtract it. When measuring delays, you must subtract the delay of the test-access path to the input of the circuit under test from the delay to the output to ensure that the access path's delay cancels. ATE often uses both multiplication and subtraction to perform analog self-calibration, but this operation requires too much circuitry to be economical for BIST. Low-frequency effects can appear as fluctuating systematic errors, such as an offset that changes at 50 or 60 Hz because of power-line noise.

You can improve precision by adding samples to compute an average. Random noise in a signal or in the measurement circuitry limits the repeatability of any measurement of the signal's properties. As you include more samples in a measurement, the test variance and repeatability improve. Analog-measurement circuitry typically accomplishes averaging with lowpass filtering or charge integration in a capacitor.

You can use full adders in analog BIST's digital circuitry, but, in many cases, you can more efficiently accomplish averaging with binary counters. You cannot cancel noise that is not random, such as interference from nearby synchronous logic or 60-Hz power, by simple averaging or subtraction. You can, however, reduce its impact by sampling synchronously to the interference (**Reference 1**) or by integrating for an integer number of cycles of the interfering frequency.

To be cost-effective, BIST circuitry must have higher yield than the circuit under test. In the case of digital BIST, this requirement means simply that its area must be smaller than that of the circuit under test. For analog BIST, however, this principle also means that the BIST must achieve its required linearity, noise, and bandwidth without affecting yield. In a case study, only 70% of small analog-BIST circuits on a test chip achieved the required measurement accuracy. This BIST's yield impact on an SOC (system on chip) would be the same as a circuit occupying 30% of the whole SOC.

The best way to implement BIST so that it has higher yield than an analog circuit under test is to minimize the amount of analog circuitry in the BIST—that is, make it digital. You can reduce the relative area of BIST circuitry by sharing one BIST circuit among many functions. Digital BIST can easily achieve this task, but analog BIST cannot because of the diversity of functions requiring testing. Such was the reasoning behind MadBIST, a scheme that MF Toner and Gordon W Roberts developed (**Reference 2**). In MadBIST, one DSP first tested an ADC and then a DAC. MadBIST, the ADC, and the DAC then tested other analog circuitry.

A problem with using a shared analysis block is conveying the analog signal of interest to the block. Analog busses commonly perform this task, but they introduce loading, noise, and nonlinearity, and they reduce bandwidth. An alternative is to locally convert the signal to some form of digital representation and then use a digital bus.

Analog BIST must be able to apply specification-based structural tests. In other words, the applied stimulus and response analysis must permit correlation of the results with the analog circuit's functional specifications, but they must also target manufacturing defects to facilitate diagnosis and minimize test time. Defect-oriented testing strives to accomplish this task but does not normally try to use function-like tests. Philips (now NXP) in 1995 first performed one of the few published industrial comparisons between conventional specification-based analog testing and defect-oriented test (**Reference 3**). It concluded that defect-oriented test achieved faster testing for similar defect coverage when the design specifications had significant margin and the process was well-controlled. Otherwise, specification-based testing was necessary for maintaining test coverage and yield.

DIGITAL BIST INHERENTLY APPLIES A FUNCTIONLIKE STIMULUS BECAUSE ALMOST ANY PATTERN OF ONES AND ZEROS REPRESENTS THE INPUT SIGNALS IN FUNCTION MODE.

Digital BIST inherently applies a functionlike stimulus because almost any pattern of ones and zeros represents the input signals in function mode, including pseudorandom data. Delivering a functionlike stimulus to an analog circuit can be more complex. Pseudorandom noise is an enticing analog stimulus that addresses many potential defects and is easy to generate. A resistor and a capacitor can filter the output of the LFSR in digital BIST to produce an analog waveform. Multipliers and adders can cross-correlate the response of the analog circuit under test to its pseudorandom input.

Another more easily implemented approach is to reconfigure the circuit into an oscillator by connecting its output to its input, adding gain or inversion if necessary, and measuring the resulting oscillation frequency. The technique is area-efficient. Unfortunately for both these approaches, determining whether the circuit under test meets specifications has proved difficult because the measurement is too insensitive

to noise and nonlinearity, and diagnosis is impractical.

ATE widely uses a linear ramp and a single-tone sine wave as test stimuli to efficiently test linearity and aid diagnosis of ADCs and DACs. The most robust way to generate a pure ramp or sine on-chip is to store a periodic sigma-delta bit stream in a circulating shift register, though this approach may require thousands of logic gates plus analog filtering. Fortunately, one stimulus block may be sufficient for all analog functions in an SOC and can efficiently convey the serial digital bit stream to all areas of a chip.

The easiest useful stimulus to generate is a digital square wave, which you can use to test a step or an impulse response. Surprisingly, an accurate dc voltage is a difficult stimulus or reference for a sampling comparator to generate unless you resort to analog techniques that require more self-test. Lowpass filtering of a programmable-duty-cycle digital waveform produces a mostly dc waveform for which the average voltage depends on the duty cycle and, at high switching frequencies, on the mismatch in the rise and fall times of the digital signal.

Reducing the switching frequency reduces the dc voltage's sensitivity to this mismatch but increases the peak-to-peak variation of the dc voltage. In analog functions, such as voltage regulators, additional active lowpass filtering reduces this noise. Analog BIST using this approach must test the filtering, however. A technique that is more suitable for BIST was recently presented at the Workshop on Test and Verification of High-Speed Analog Circuits (**Reference 4**).

The last principle of analog BIST is that it must output its result as a digital measurement and its pass/fail bits resulting from comparison to upper and lower test limits. An analog-voltage result would be subject to corruption if you conveyed it off-chip for characterization and would require mixed-signal ATE. A digital result, without on-chip comparison to limits, would require the ATE to capture and analyze digital words instead of single bits, preventing the use of the most common test-pattern languages, WGL (waveform-generation language) and STIL (Standard Test Interface Language), and many low-cost testers. A pass/fail result alone would prevent characterization of parameters and measurement repeatability, which is an essential step toward setting test limits.

PLL-BIST ACCURACY?

Taking a look at these essential principles helps answer the PLL designer's question. Practical PLL BIST uses neither analog circuitry nor delay lines, making it less sensitive to noise than the PLL under test. PLLs must generate a low-jitter edge every nanosecond, for example, and minimize jitter accumulation. However, PLL BIST can undersample edges using a pretested low-jitter clock conveyed through a few digital inverters that have fast transitions to minimize added jitter.

If a pretested clock is not available, then one PLL can sample the edges of another PLL on the same chip, operating at a slightly asynchronous frequency. The resulting jitter measurement is the sum of the two jitter levels; random jitters cannot cancel each other. Adding many such samples in a histogram reduces the impact of spurious noise, and sampling at the same rate as any interference can further reduce this impact.

THE NEED FOR ANALOG BIST

Few analog-BIST techniques that anyone has proposed in the past 15 years embody all of the principles noted here. Yet all of these principles are essential for the BIST to be practical and cost-effective. Developing a practical analog BIST has proved perhaps too challenging, but engineers will undoubtedly develop techniques that embody these principles because the need for them is increasing.

SOCs are including more system analog functions and higher pin and higher gate counts, all of which drive up tester costs and test times. The addition of embedded flash memories can greatly increase test time—to more than a minute—making multisite test essential, and this requirement drives the need for low-pin-count access and more analog test resources.

A significant roadblock that prevents adoption of analog BIST or any other new analog-test technique is the lack of an industry-accepted analog fault model. Fortunately, one outcome of a panel discussion at the 2009 International Test Conference (**Reference 5**) is that several of the panelists expressed interest in developing an IEEE-sponsored standard analog fault model. The panelists also agreed that more DFT (design-for-test) automation is necessary before the industry can adopt any new technique—a scenario that has happened for the digital portions of ICs. EDA companies can develop automation only when IC designers adopt systematic general techniques that can test many functions on an IC. EDN

REFERENCES

1 Sunter, Stephen, and Aubin Roy, "Noise-Insensitive Digital BIST for any PLL or DLL," *Journal of Electronic Testing: Theory and Applications*, Volume 24, No. 5, pg 461, October 2008, http://bit.ly/cl5phj.

2 Toner, MF, and Gordon W Roberts, "A BIST Scheme for an SNR Test of a Sigma-Delta ADC," *Proceedings of the International Test Conference*, October 1993, http://bit.ly/dfG2oR.

3 Sachdev, Manoj, "A Realistic Defect Oriented Testability Methodology for Analog Circuits," *Journal of Electronic Testing: Theory and Applications*, Volume 6, No. 3, pg 265, June 1995, http://bit.ly/bDjjnc.

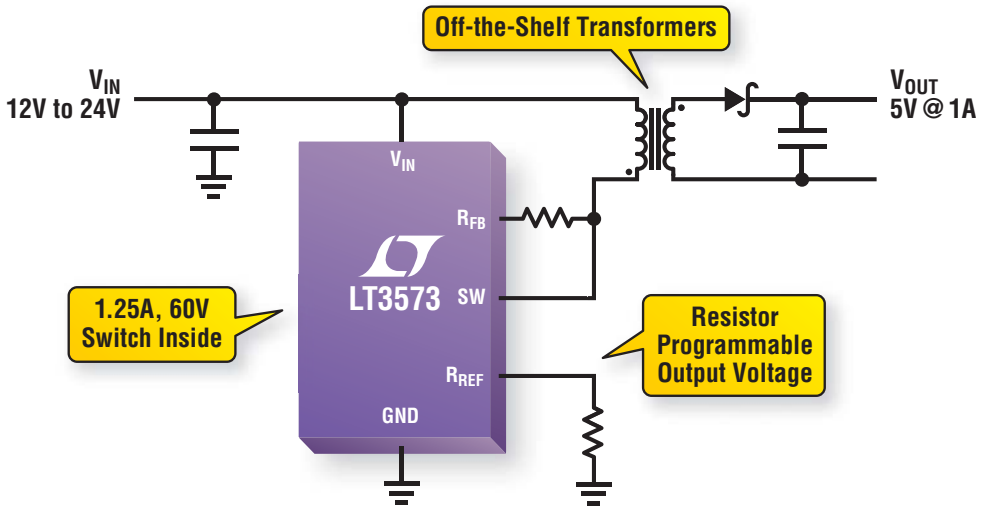
4 Sunter, Stephen, "A General Strategy for BIST of High-Speed Analog Functions," *Informal Digest of Workshop on Test and Verification of High-Speed Analog Circuits*, November 2009.

5 Wilson, Ron, "ITC 2009 panel explores future of analog test," *Test & Measurement World*, November 2009, http://bit.ly/aEL29C.

AUTHOR'S BIOGRAPHY

Steve Sunter is the engineering director for mixed-signal DFT with the Mentor Graphics silicon-test-solutions division. He has published dozens of papers, of which three won awards, and four book chapters on mixed-signal DFT; received 25 US patents in the area; and for three years served as chairman of the International Mixed-Signal Testing Workshop. Sunter has a bachelor's degree in electrical engineering from the University of Waterloo (Waterloo, ON, Canada).

Isolated Flyback–No Opto



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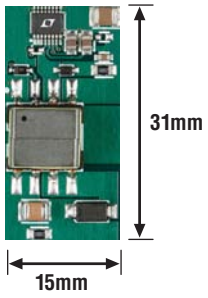

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READERS SOLVE DESIGN PROBLEMS

Circuit achieves constant current over wide range of terminal voltages

Donald Boughton, Jr, International Rectifier, Orlando, FL

Analog-circuit design often requires a constant-current sink. An example would be for a TRIAC (triode-for-alternating current) dimmer holding current in fluorescent or solid-state lighting. Other examples include a precise current sink at the end of a long line, such as a cable or an ADSL (asymmetric digital-subscriber-line) modem, which produces a "signature" current value that alerts the device at the source end, such as an exchange office or a cable center, that the remote equipment is attached. The trick is to make a circuit that gives a constant current over a variety of terminal voltages.

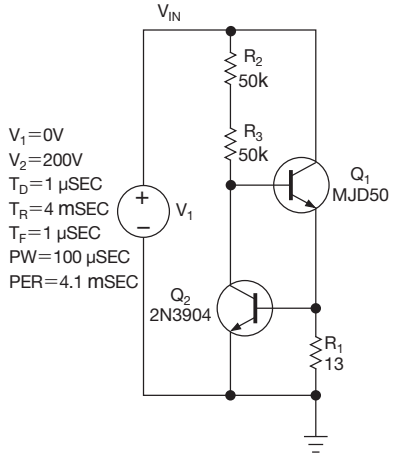

Figure 1 Resistor R_1 sets a constant current through Q_1.

A common circuit for achieving this task uses a sense resistor, a transistor, and a power device. **Figure 1** shows the circuit using a power transistor, Q_1. The circuit provides an approximate constant current at high voltages, but it doesn't enter regulation until it reaches nearly 60V due to the base current the transistor requires. **Figure 2** shows the circuit using a MOSFET, Q_2, for the power device. With a MOSFET, you can use smaller biasing resistors, and the circuit comes into regulation at a much lower terminal voltage.

Unfortunately, the current-sense resistor, R_1, in **figures 1** and **2** doesn't sense the bias current. As the terminal voltage increases, the terminal current also increases because of the increased bias current. A simple way to improve the regulation of both circuits is to add re-

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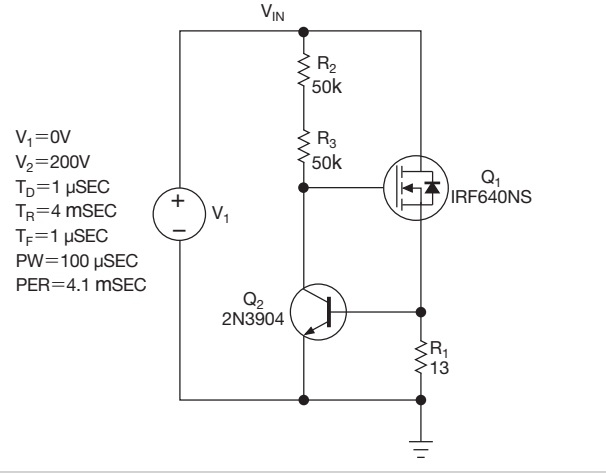

Figure 2 This circuit substitutes a MOSFET for Q_1 in Figure 1 and uses smaller resistors.

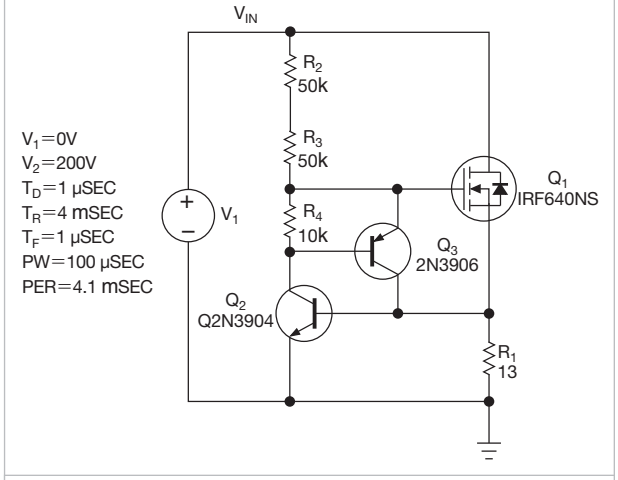

Figure 3 The addition of Q_3 and R_4 improves current regulation.

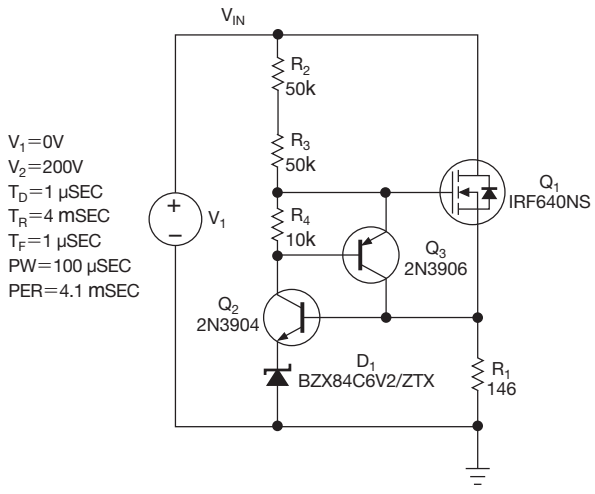

Figure 4 Adding a zener diode improves current regulation over temperature.

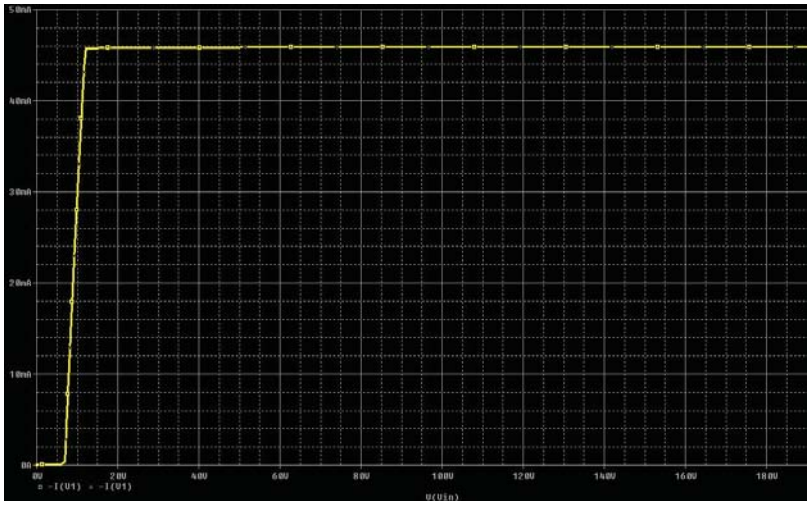

Figure 5 A constant current in Q_1 has a steep rise relative to V_{IN}.

sistor R_4 and PNP transistor Q_3 (**Figure 3**). R_4 and Q_3 form a constant-current source to the collector of Q_2. The circuit diverts any excess bias current through the collector of Q_3 to sense resistor R_1. Thus, as the terminal voltage increases, the bias current remains relatively constant, and the current regulation appears much flatter.

The negative temperature coefficient of the base-to-emitter junction of transistor Q_2 causes another problem with this kind of circuit. The temperature coefficient is approximately –1.6 mV/°C, which causes the current value to vary widely with temperature.

A 100-mV CHANGE WITH TEMPERATURE DOES NOT SERIOUSLY AFFECT THE REGULATED CURRENT.

One way to approach this problem is to add a 6.2V zener diode, D_1, in series with the emitter of Q_2, which increases the sense voltage (**Figure 4**). A 6.2V diode has a positive temperature coefficient, which counteracts the negative temperature coefficient of the transistor. Furthermore, the total sense voltage is much larger, so 100 mV or so of voltage change with temperature does not seriously affect the regulated current. **Figure 5** shows a PSpice simulation of the circuit that uses a MOSFET for Q_1. EDN

Limit inrush current in low- to medium-power applications

JB Castro-Miguens, Cesinel, Madrid, Spain
C Castro-Miguens, University of Vigo, Vigo, Spain

When switched-mode power supplies, including those for notebook computers, turn on, the bulk capacitor of the uncontrolled rectifier is completely discharged. This can result in a large charging current for a high instantaneous line voltage because the discharged capacitor temporarily short-circuits the power supply's diode bridge.

With a large bulk capacitor, the current spike can trigger the mains breaker or even destroy rectifier diodes. Capacitor and line ESRs (equivalent series resistances) and inductances help to reduce the initial spike. Even so, current peak can reach tens of amperes. The rectifier-diode selection must account for this nonrepetitive spike. An initial spike also affects the lifetime of the bulk capacitor. The circuit in **Figure 1** lets you avoid the large initial spike.

At turn-on, if the instantaneous rectified ac-line voltage is greater than about 14V, MOSFET Q_1 is on, ensuring that IGBT (insulated-gate bipolar transistor) Q_2 is off. In this situation, no current flows through charging the bulk capacitor.

Whenever the rectified ac-line voltage is lower than the voltage across the bulk capacitor plus approximately 14V ($V_1=V_{IN}–V_{OUT}\leq 14V$), Q_1 is off, and Q_2

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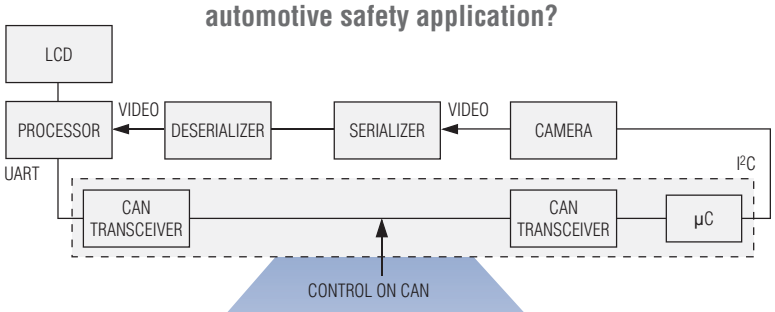

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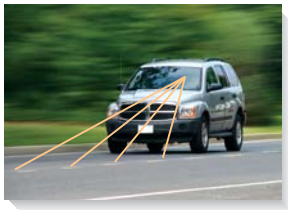

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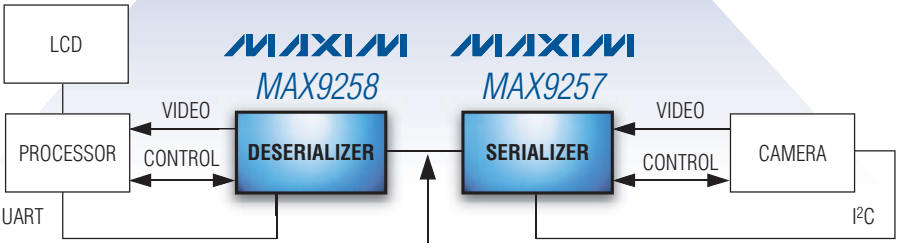

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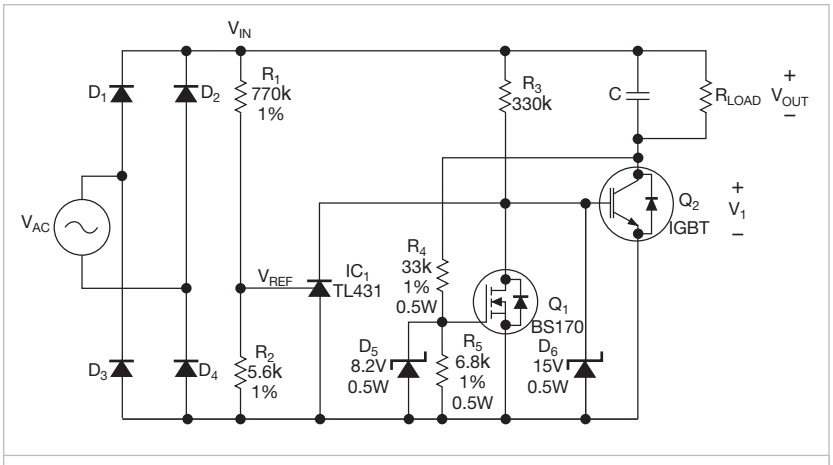

Figure 1 You can use this circuit to limit inrush current and clamp the output voltage to values lower than 380V.

turns on through R_3, connecting the capacitor and R_{LOAD} to the rectifier. Q_2 remains on thereafter, making Q_1 useless.

In the steady state, whenever the rectified input ac voltage matches the voltage across the bulk capacitor, Q_1 is off and Q_2 is on, making charging of the capacitor possible.

The current-limiting circuit lets you implement straightforward overvoltage protection. When the rectified output voltage is higher than 380V, the reference-to-anode voltage of IC_1 is higher than its internal reference of 2.495V, making the anode-to-cathode voltage drop to approximately 2V. In this situation, the cathode sinks the current across R_3, turning off Q_2.

When the rectified line voltage is lower than 380V, the cathode current of the TL431 is approximately 0A. Thus, Q_2 turns on through R_3, connecting bulk capacitor C and R_{LOAD} to the full-wave rectifier if $V_1=V_{IN}-V_{OUT}\leq 14V$.

All the components have a small power dissipation. The GP10NC60KD transistor, with an input of 230V rms and a load as high as 500W, is suitable for Q_2. EDN

Electronically tinge white-light source

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

White-light LEDs are becoming commonplace in everyday life. A classic white LED is an InGaN (indium-gallium-nitride) LED, emitting spectrally "pure" blue light. Photoluminescence spreads the spectrum of these LEDs and converts it into a light resembling daylight. This conversion takes place in a layer of yellow ZnSe (zinc selenide), which covers the InGaN chip. Due to production tolerances in the thickness of the ZnSe layer, these white LEDs are available in yellowish warm-white, neutral, and slightly bluish cool-white grades. To derive another hue from a white-light source, you can use the LED driver circuit in **Figure 1**.

The light source, IC_1, is an Avago Technologies (www.avagotech.com) ASMT-MT00 RGB (red/green/blue) LED. The driver contains two resistive DACs, IC_3 and IC_5, which function as potentiometers (**Reference 1**). The DAC's preset pins, PRE1 and PRE2, are grounded. Both resistive DACs are therefore set to midscale after power-on.

The true midscale for the IC_3 DAC at its wiper pin is one-third scale for IC_3, set by the resistor $R_{SH}=R_{A1B1}/2$, where R_{A1B1} is the resistance between the ends of the potentiometer. Voltage follower IC_{8A} ensures that the voltage at potentiometer IC_3 remains a constant reference voltage regardless of the position of wiper P_1. Voltage follower IC_{8A} is necessary because the resistance between the A1 and B1 terminals of IC_3 varies from 10 kΩ for wiper P_1, when grounded, to 3.33 kΩ for the A1 position of P_1. In this way, the drivers for the red, green, and blue LEDs generate the same value of current of $V_{REF}/3R_F$, where V_{REF} is the reference voltage. Thus, you get white light at power-on.

If you require, for example, a pale-pink hue, you ground the $\overline{PD1}$ pin for a short period. Wiper P_1 thus moves down by one step, decreasing the content of green light in the resulting light while increasing the contents from the red and blue LEDs. The sum of the I_R, I_G, and I_B currents remains constant, regardless of the positions of wipers P_1 and P_2. The luminous intensity of the output light holds constant. Any further short-term grounding of the $\overline{PD1}$ pin leads to a deeper violet hue of the output light. To get turquoise or bluish-green-tinted white light, you simply ground the $\overline{PD2}$ pin for short periods. The relative content of the red component then decreases below one-third of full-scale. If you ground the $\overline{PU1}$, $\overline{PD1}$, $\overline{PU2}$, or $\overline{PD2}$ pins for short periods, you can arbitrarily set hues of the light. The color resolution comes from adding or removing current in approximately 3% steps while removing or adding an equal number of approximately 3% steps of the remaining basic color components. A 100% step equals the total light intensity, regardless of color. This intensity is constant because the sum of currents flowing through the red, green, and blue LEDs is constant and has a value of V_{REF}/R_F. The resistive DACs have wiper-position margins.

The zero-scale relative margin is typically 1% of full-scale. The upper-position relative margin, or margin of the upper value of resistance between the B and the wiper terminals, is δ_V=2.4% of full-scale. Resistor R_{SH} artificially increases the upper margin of the V_{OUTG} voltage. The following **equation** yields the maximum settable voltage for V_{OUTG}:

$$V_{OUTGMAX}\simeq\frac{1}{1+3\delta_V}\times V_{REF}$$
$$\simeq(1-3\delta_V)\times V_{REF}.$$

By evaluating the **equation**, you determine you can set 92.8% green and subdivide the remaining 7.2% between the red and blue components by grounding $\overline{PU1}$ for a long time. If you also ground the $\overline{PU2}$ pin for more than 4 seconds, you get a yellowish- or warm-green color. In contrast, if you ground the $\overline{PD2}$ pin for more than 4 seconds, you get aqua or a cool-green color. Thus, changing even a moderate 7.2% of basic components of the light results in highly discernible hues.

Paralleling the R_{SH} between the B1 and P_1 terminals of resistive DAC IC_3 causes these terminals to exhibit nonlinear behavior. The step change of voltage at wiper P_1 decreases to two-thirds at the midscale of IC_3 and gradually rises when moving the wiper from the midscale toward zero. At zero, this step change recovers fully to its original relative value of 1/32. When moving P_1 from midscale toward full-scale, the step change rises and triples to a value of 3/32 at full-scale. This nonlinear behavior has, however, no detrimental effects. In contrast, close to the midscale, it makes the resolution 1.5 times that of the resistive DAC alone. EDN

REFERENCE

1 Štofka, Marián, "Set LEDs' hue from red to green," *EDN*, Oct 21, 2010, pg 59, http://bit.ly/a96DXg.

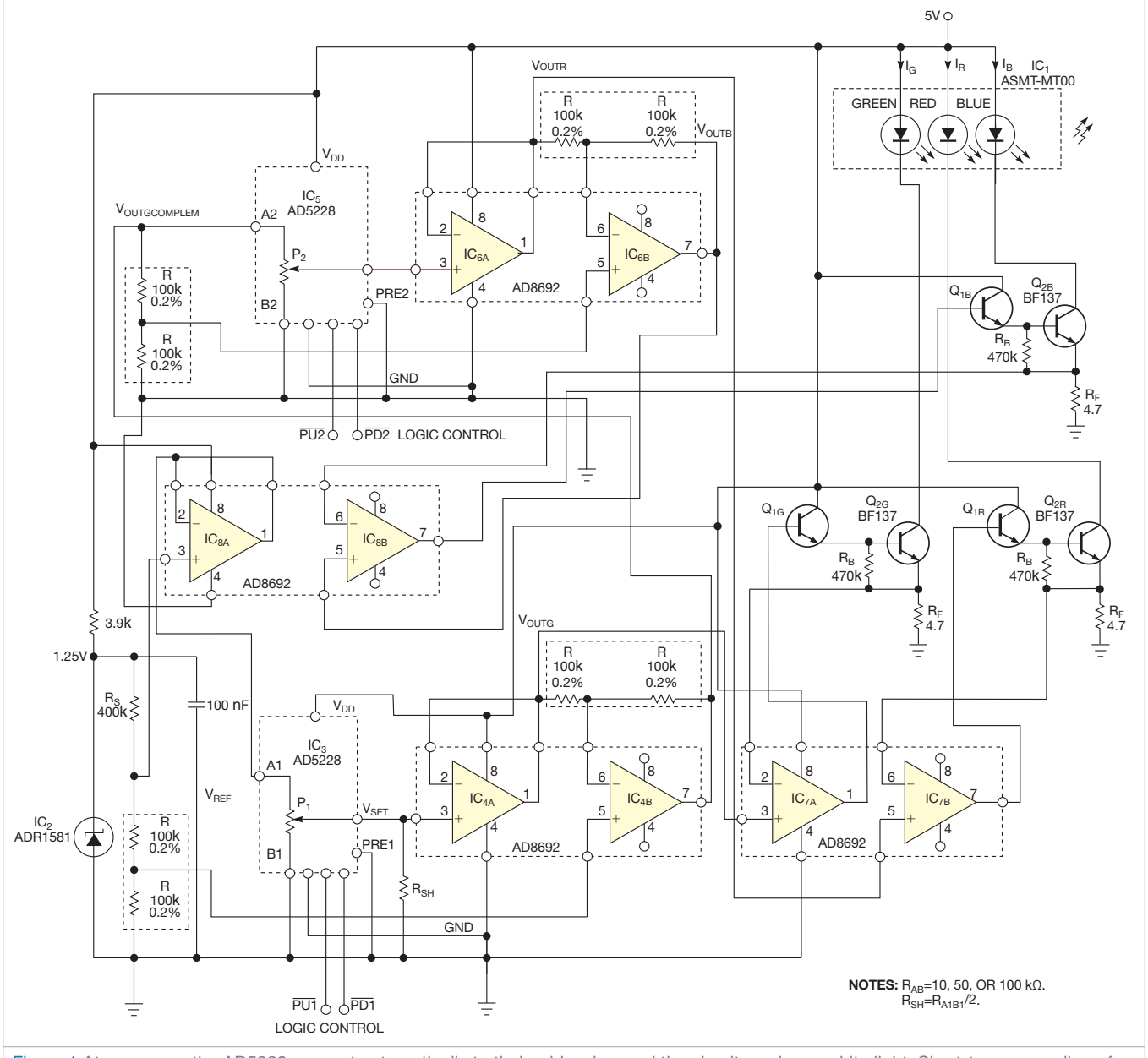

Figure 1 At power-up, the AD5228s are set automatically to their midscales, and the circuit produces white light. Short-term grounding of four control pins lets you tinge the light while holding intensity constant.

Transistor boosts regulator current

Yngve Linder, Örsundsbro, Sweden

Some circuits require a constant-current source that doesn't necessarily connect to a power-supply rail or to ground. The circuit in **Figure 1** shows a simple method for achieving that configuration.

The LM317 voltage regulator develops 1.25V between the OUT and the ADJ pins. Placing a resistor between those pins produces a constant current. Thus, the circuit's output current is $1.25V/R_{ADJ}$. The transistor lets the circuit source more current than the regulator alone can provide once the current through R_1 creates enough voltage to turn the transistor on. Otherwise, the regulator supplies the load current. EDN

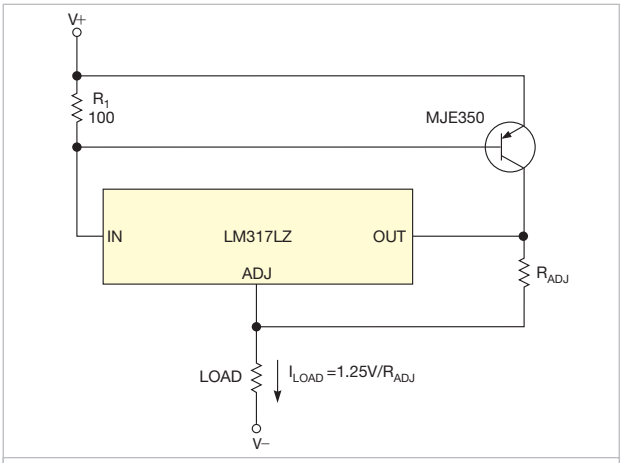

Figure 1 This simple method achieves a constant-current source that doesn't necessarily connect to a power-supply rail or to ground.

Detect live ac-mains lines

Raju R Baddi, Raman Research Institute, Bangalore, India

You can use a simple battery-powered circuit to detect whether an ac-mains wire is live without making any electrical contact with it. The circuit uses a CD4011 NAND gate's high input impedance to sense a magnetic field from a 50- or 60-Hz ac-mains line. You simply bring the detector coil near the socket to see whether it has a proper ac connection. If it does, then the LED will illuminate (**Figure 1**).

The detector in this case is a coil of copper wire. When you place it near a live wire carrying ac current, the coil develops a voltage across the CD4011 at pins 1 and 2. This voltage produces square waves at the output of the gate, driving the LED active. In the absence of any hot ac wire near the detector plate, the 1N4148 diode connected to the first gate's inputs keeps the gate biased. This bias ensures that, under normal conditions, the final output from the gates is low, keeping the LED off.

Placing the detector plate close to a live wire sets up an oscillating voltage at the gate's input at pins 1 and 2. That voltage produces square waves corresponding to the ac-mains frequency. The remaining three gates of CD4011 connect in parallel, which increases the current through the LED enough to light it.

A rechargeable, 3.6V nickel-cadmium battery powers the circuit. You can assemble the detector into a convenient, pocket-sized glue-stick tube (**Figure 2**). The circuit consumes nearly no power when the indicator LED is off. Thus, you can also power the circuit using lithium cells, such as the popular CR2032. EDN

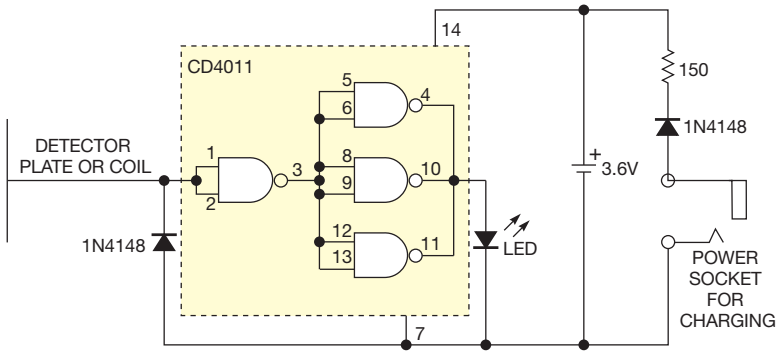

Figure 1 A battery-powered live-wire detector lights an LED in the presence of a field.

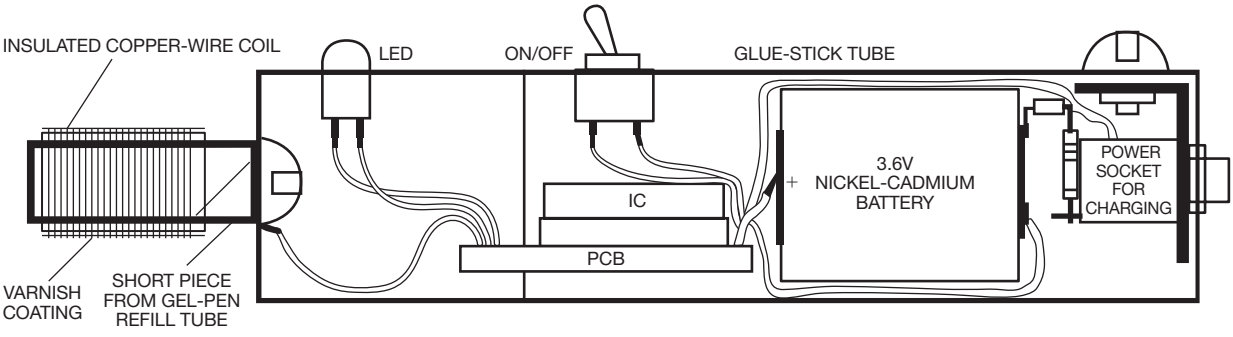

Figure 2 The circuit can fit into an empty tube of glue. Be sure to varnish the coil for best performance.

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Patchwork of state e-waste laws keeps expanding

Currently, 23 states have passed laws regulating e (electronic)-waste, further challenging design and end products. Each state has its own criteria for disposing of discarded electronic products, and each has its own registration process, a burden on OEMs. There are perennial attempts at national legislation that would create one set of rules, thus making compliance simpler and less costly, but no bill is likely to pass soon. Even if a federal bill were to gain traction, there is no guarantee that it would pre-empt state regulations and could end up as just one more conflicting regulation.

Although e-waste sits at the opposite end of the product life cycle from design, the ramifications of state e-waste laws are hitting the design community. Many states are taking the liberty of packing e-waste regulation with EU (European Union) ROHS (restriction-of-hazardous-substances)-like restrictions on materials. "Starting in January 2011, you can't sell anything in New Jersey that includes materials banned in the European Union," says Ken Stanvick (**photo**), vice president and co-founder of Design Chain Associates (www.designchainassociates.com), which advises OEMs and suppliers on environmental compliance. "Minnesota wants a notice [about] whether you are … ROHS-compliant. These laws are only going to get more inclusive in adding materials restrictions."

The electronics-industry OEMs that sell globally most likely are now ROHS-compliant because the regulation has been in effect for years. However, the state e-waste laws may force companies in the aerospace, military, and medical-device industries that sell only in North America into ROHS compliance.

Another impact on design will come in the form of designing for easy disassembly. "Some products have a soldered battery to avoid handle vibration," says Stanvick. "The European Union has tried to address this [problem] to make sure that design doesn't cause undue work in recycling. The [European Union is] talking about having battery holders for easy reuse." Because many of the e-waste laws in the United States are taking their model from Europe, Stanvick expects these concerns to find their way into the state e-waste laws. Stanvick also points to plastics as concerns for design. He expects states to pressure OEMs to include easy-to-recycle plastics in their product designs.

The conflicting state regulations have made compliance difficult for OEMs. "It's a real challenge to comply with 23 requirements," says Rick Goss, vice president of environment and sustainability at the ITIC (Information Technology Industry Council, www.itic.org). "The registration process alone is confusing." Goss also notes that, although fewer than half the states have e-waste laws, those states with regulations represent two-thirds of the US population.

As an example of the conflicting laws, Michigan recently passed regulation that established no mandatory collection goals. Instead, the state has asked manufacturers to voluntarily collect an amount equaling 60% of the weight of the products they sell in the state. Minnesota, however, asks manufacturers to recycle a set number of pounds based on the sales weight of video-display devices but can count a larger array of products, such as computers, DVD players, and printers, toward meeting that goal.

Reactions to e-waste bills have been mixed. Some industry stakeholders are not eager to revive efforts to produce and push a federal bill. "In the federal end, there seems to be little appetite for any federal recycling infrastructure," says the ITIC's Goss. Still, some industry groups push on for a unifying solution.

Read more on this topic at www.edn.com/101104sc.

—by Rob Spiegel

ASIA RECEIVES DUMPED E-WASTE

Another problem coming out of the move toward e-waste regulation is the states' inability to control what happens to e-waste once it's collected. Manufacturers are illegally selling a large portion of the e-waste in bulk in Asia and West Africa. "States are not allowed to establish export controls," says Rick Goss, vice president of environment and sustainability at the Information Technology Industry Council. "So states are looking to see the federal government step in on e-waste exports. Brokers and exporters engage in these illegal activities." Goss notes that Europe faces that same problem with lax enforcement of e-waste exports from European ports.

The practice of disassembling e-waste is costly in human terms. "Families are trying to recover metals from the board. They use acid to take off the metals, and there are a lot of stories about its ruining the environment. Plus, there's child labor involved," says Ken Stanvick, vice president and co-founder of Design Chain Associates. "It's out of sight, out of mind, and China turns a blind eye to it."

For more on inadequately controlled e-waste recycling, see "E-waste tragedy: What can be done?" http://bit.ly/bnBMiP.

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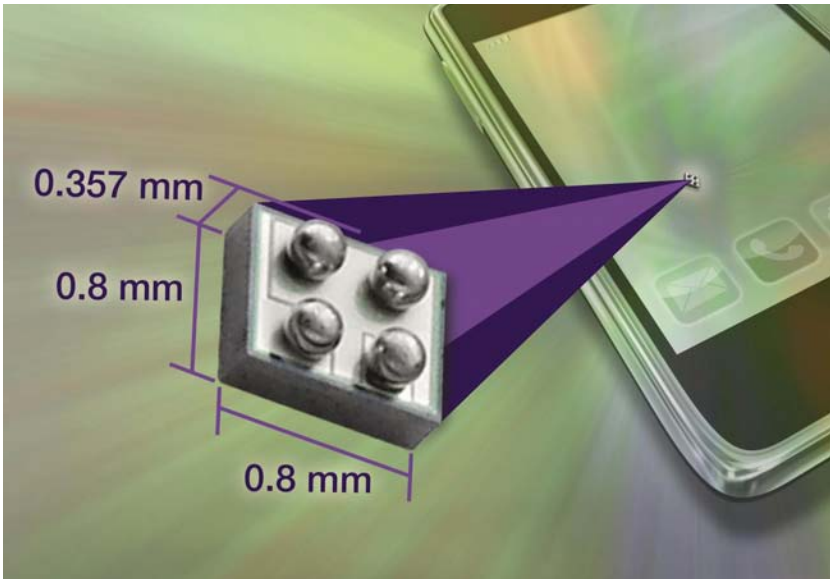

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Vishay Siliconix, www.vishay.com

Dual 70V, 15-mA Schottky diode comes in SOT-963 packages

The dual-isolated 70V, 15-mA CMRD6263DO Schottky diode comes in an ultraminiature SOT-963 surface-mount case. The device has a forward voltage of 395 mV and a switching speed of less than 395 mV. Designers can arrange the device in a variety of configurations, including common anode, common cathode, or in series using the suggested alternative mounting-pad geometries. The device can also work in full-wave-bridge configurations. Prices for the CMRD6263DO start at 14 cents (8000) on tape and reel.

Central Semiconductor Corp, www.centralsemi.com

High-voltage gate-driver ICs target motor, industrial applications

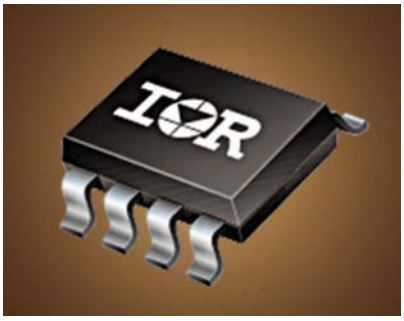
This family of gate-driver ICs includes the two-input, two-output FAN7392 high- and low-side driver; the one-input, two-output FAN7393 half-bridge driver with shutdown and controllable dead time; the one-input, two-output FAN73932 half-bridge driver with shutdown and fixed dead-time control; and the two-input, two-output FAN73933 half-bridge driver with controllable dead time. The devices feature a common-mode dV/dt noise-canceling circuit that enables stable operation of the high-voltage gate driver under high dV/dt-noise circumstances. The devices also feature an advanced level-shift circuit that offers

high-side gate-driver operation with negative floating-supply-voltage swings as high as –9.8V at a high-side floating-supply voltage of 15V. The devices operate at a temperature range of –40 to +125°C and sell for $1.52 (1000) each.

Fairchild Semiconductor, www.fairchildsemi.com

–30V P-channel power MOSFETs target battery-charge and -discharge switches

The –30V IRF9310 P-channel MOSFET comes in an SO-8 package and targets use in battery-charge and -discharge switches and system and load switches in dc applications. The devices feature a 4.6 to 59-mΩ on-resistance to match a range of power requirements. P-channel MOSFETs also eliminate the need for



level-shifting or charge-pump circuitry. Prices for the IRF9310 start at 43 cents (10,000).

International Rectifier, www.irf.com

Synchronous-rectification drivers suit computing, consumer applications

The NCP4303A and NCP4303B synchronous-rectification-controller and driver ICs target use in switch-mode power supplies and secondary-side rectification in switch-mode power supplies. The devices operate at a maximum frequency of 500 kHz and have a typical turn-off-delay time of 40 nsec. The devices' adjustable on and off times, which are independent of the supply-voltage level, help with the ringing that PCB layouts and other parasitic elements induce. The NCP4303 also features a trigger input that can interface with the primary side of the power supply, allowing use in constant-current applications. The NCP4303A has a 12V gate-drive

clamp, and the NCP4303B has a 6V gate-drive clamp. The price for either device is 43 cents (10,000).

On Semiconductor, www.onsemi.com

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Bright lights, big pity

DANIEL VASCONCELLOS

Many years ago, I was the sole hardware resource at a company that developed advanced software for a government agency, so I had exposure to a wide range of hardware and problems. We were developing some early graphical interfaces that required several racks of hardware to run. The practice was to send videotapes as collateral to progress reports so that the sponsor could both see and read about the results.

Inevitably, we waited until the last moment to make the tapes so that we could show the latest improvements. This delay led to more than one tense midnight session when things did not go as well as they might have, which they never did.

We eventually had the videotape-creation sessions down to almost-controlled chaos. One important preliminary step in making the tape was to clean the heads on the ¾-in. semiprofessional-video recorder because the heads frequently became clogged and they were especially sensitive to stray tape oxide when recording.

Late one Friday afternoon, I cleaned the heads as usual, which involved an irritatingly large number of screws to remove the cover to gain access. As always, I performed a quick test before replacing the cover.

This time, the tape started to load and then the machine went into its tape-jam panic mode and ejected the tape. This situation by itself was not unusual and often was due to the use of a defective tape. I tried another tape, but I got the same result. "Things don't look good," whispered the little voice in my head at about the same time that my boss repeated his unanswered question about what was going on.

I leaned over the machine to carefully watch the loading sequence in an attempt to spot what was causing the issue. To my surprise and relief, the tape loaded perfectly. One success in three attempts was not a great record, however, so I tried again, and the tape-jam panic recurred. This situation was not at all good.

With my increasingly nervous boss at my side, I carefully watched the loading sequence, which worked flawlessly several times in a row. We relaxed, and I tried one last time before replacing the cover. Unfortunately, the tape jammed again. A programmer in the room who had been watching all this joked, "How does it know you are watching?"

THE BULB FROM THE OVERHEAD-LIGHT FIXTURE WAS STRONG ENOUGH TO FOOL ONE OF THE TAPE SENSORS AND CAUSE THE FALSE TAPE-JAM ALARM.

The remark caused me to get an idea—a light bulb over my head, just as in the iconic comic-book symbol. The machine used a number of optical interrupters, including LED and phototransistor pairs, to sense the presence or absence of a tape. By unfortunate chance, the machine sat directly under an overhead-light fixture that had recently received a new bulb. The bulb was strong enough to fool one of the tape sensors and cause the false tape-jam alarm.

Whenever we were watching closely, the light was blocked; whenever we were away from the machine, the light hit the sensor, and the false jam occurred. I replaced the cover, and all went as well as usual, which is to say we were done just before midnight.

That is not the last time the how-does-it-know-you-are-watching question has come up in my debugging career. It is, of course, just a subset of the what-did-you-recently-change question that is also useful, although that one sometimes causes much wasted time because problems don't always play by the rules. EDN

Martin Moeller is an engineer at Calix (Acton, MA).

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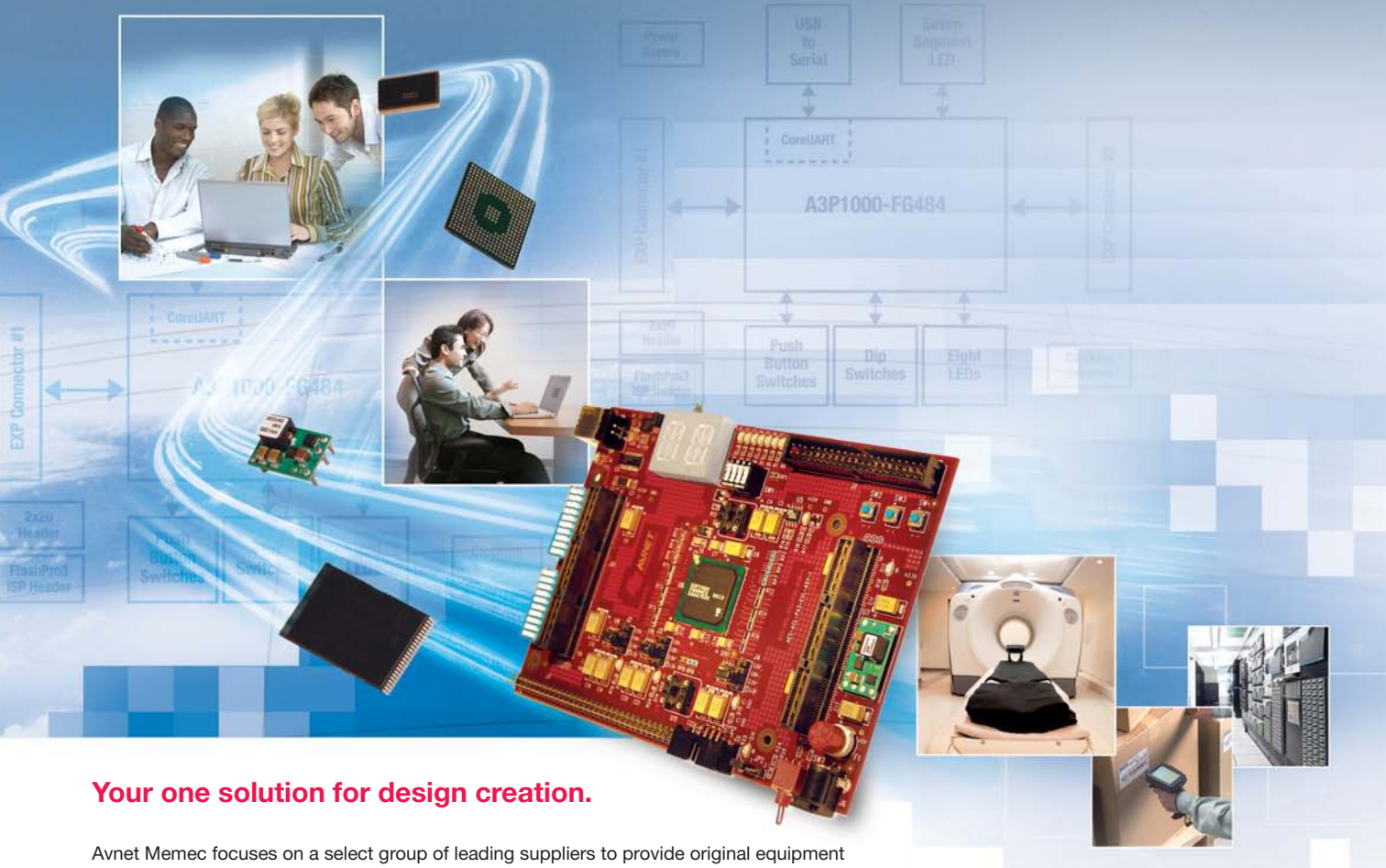

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